# RESUME (of Indrajit Chakrabarti)

## EDUCATION :

- **Ph.D.** in **Computer Science and Engineering** from Indian Institute of Technology Kharagpur, India, 1997.
- **M.E.Tel.E.** (Master of Engg. in **Electronics & Telecommunication Engg.**) from Jadavpur University, Kolkata, India 1990.
- **B.E.Tel.E.** (Bachelor of Engg. in **Electronics & Telecommunication Engg.**) from Jadavpur University, Kolkata, India 1987.

## PROFESSIONAL EXPERIENCE:

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|---|---|
| 31 Dec'2014 till date | **Professor, Department of Electronics and Electrical Communication Engineering,** Indian Institute of Technology Kharagpur, India. |
| 16 Dec'2004-30 Dec'2014 | **Associate Professor, Department of Electronics and Electrical Communication Engineering,** Indian Institute of Technology Kharagpur, India. |
| 4th June'2004-15 Dec'2004 | **Associate Professor, Department of Electronics and Communication Engineering,** Indian Institute of Technology Guwahati, India. |
| Jan.' 1998 - 3rd June'2004 | **Assistant Professor, Department of Electronics and Communication Engineering,** Indian Institute of Technology Guwahati, India. |
| Oct.'1996- Dec.'1997 | **Lecturer in Electronics and Communication Engineering,** Bengal Engineering College, Sibpur, Howrah, India. |
| Nov.'1995-Oct'.1996 | **Programmer** in Computer Centre, IIT Kharagpur, India |
| July'1987-Aug'1988 | **Electronics Engineer** in Micronics Corporation, Makhla, Hooghly, West Bengal |

## SPONSORED PROJECT:

Principal Investigator: **Dr. Indrajit Chakrabarti**
Co-Principal Investigators: **Dr. Anindya S. Dhar**
**Project Title**: ***Implementing a Scalable Video Transcoder based on Motion Compensated Temporal Filtering (MCTF)***
**Sponsor:** ISRO, Govt. of India.
**Total Cost:** Rs. 21 lakh.
**Project Duration:** October 2013 - October 2016
**Status:** Ongoing

Principal Investigator: **Dr. Indrajit Chakrabarti**
Co-Principal Investigators: **Dr. Md. Rezaul Karim** (College of Medicine Sagar Datta Hospital Kolkata) and **Dr. Sumit Chakraborty** (IPGMER and SSKM Hospital Kolkata)
**Project Title**: ***Hardware Test bed for Automated Breast Cancer Detection from Ultrasound Images***
**Sponsor:** MHRD, Govt. of India.
**Total Cost:** Rs. 30.5 lakh.
**Project Duration:** 31 March 2014 – 30 March 2017
**Status:** Ongoing

Co-Principal Investigator: **Dr. Indrajit Chakrabarti.**
Principal Investigator: **Dr. Gautam Saha**
**Project Title**: ***Development of Digital Electronic Circuits Virtual Laboratory***
**Sponsor:** Ministry of Human Resources Development, Govt. of India.
**Total Cost:** Rs. 50 lakh.
**Project Duration:** April 2010 - March 2012.
**Status:** Ongoing

Co-Principal Investigator: **Dr. Indrajit Chakrabarti.**
Principal Investigator: **Dr. Suvra Sekhar Das**
**Project Title**: ***Development of Interference Mitigation methods through Base Station Cooperation in Next Generation Wireless Broadband Mobile Communication Networks***
**Sponsor:** MCIT, DIT, Govt. of India.
**Total Cost:** Rs. 90.6 lakh.
**Project Duration:** April 2012 - March 2014.
**Status:** Ongoing

Principal Investigator: **Dr. Indrajit Chakrabarti.**
**Project Title**: ***Development of VLSI Architectures for Digital Signal Processing Algorithms***
**Sponsor:** Ministry of Human Resources Development, Govt. of India.
**Total Cost:** Rs. 8 lakh.
**Project Duration:** April 2000 - December 2002.
**Status:** Completed

**Subjects taught** (so far in IIT Kharagpur) :

(1) Digital Electronic Circuits (theory and laboratory), (2) Basic Electronics (theory and laboratory), (3) Digital VLSI Circuits, (4) Electronic Design Automation, (4) VLSI Engineering (theory and laboratory), (5) Analog Electronics (laboratory), (6) VLSI CAD (theory and laboratory)

**Subjects taught** (IIT Guwahati):

(1) IC Technology and Design (theory and laboratory), (2) Digital Electronic Circuits (theory and laboratory), (3) Analog Electronic Circuits (theory), (4) Semiconductor Devices (theory), (5) Digital Systems Design (theory), (6) Signals and Systems (theory), (7) DSP Architectures (laboratory)

**RESEARCH FIELD**: VLSI Architectures for (i) Video and Image Processing, (ii) Error Control Codes and (iii) Telecommunication

**Patent Filed:**

1. Title: System for Motion Estimation in Video Signals for Real Time Video Processing; filed on 20/08/2014 at Patent Office, Kolkata (Ref: 2029/ASA/PP-1547/iikgp, Application No.: 859/KOL/2014)

2. Title: System for Efficient VLSI Architectures for Adaptive Motion Estimation; filed on 30/04/2015 at Patent Office, Kolkata (Ref: 2235/ASA/PP-1703/IIT,Kgp, Application No.: 484/KOL/2015)

**PUBLICATIONS**: Book: 1; Journal papers: 31; Conference Papers: 67.

**Book:** Indrajit Chakrabarti, Kota Naga Srinivasarao Batta and Sumit Kumar Chatterjee, "Motion Estimation for Video Coding: Efficient Algorithms and Architectures", publisher: *Springer*, Studies in Computational Intelligence Vol. 590, January, 2015.

**1. Publications in refereed journals (details):**

(i) Rohan Mukherjee, Vikrant Mahajan, Anindya Sundar Dhar and Indrajit Chakrabarti, "High Performance VLSI Design of Diamond Search Algorithm for Fast Motion Estimation", *World Scientific Journal of Circuits, Systems and Computers*, Vol. 25, No. 9, 1650114 (16 pages), DOI: 10.1142/S0218126616501140, published online: 12 May 2016.

(ii) Rohan Mukherjee, Baishik Biswas, Indrajit Chakrabarti, Pranab Kumar Dutta and Ajoy Kumar Ray, "Efficient VLSI design of adaptive rood pattern search algorithm for motion estimation of high definition videos", *Elsevier Microprocessors and Microsystems* (2016), http://dx.doi.org/10.1016/j.micpro.2016.04.003, published online: 21st April 2016.

(iii) Rohan Mukherjee, Baishik Biswas, Indrajit Chakrabarti, Pranab Kumar Dutta, Somnath Sengupta and Ajoy Kumar Ray, "Speed-Area Optimized VLSI Architecture of Hexagonal Search Algorithm for Motion Estimation of 512x5212 Frames", *Springer Circuits Systems and Signal Processing*, DOI:10.1007/s00034-016-0315-6, published online: 23rd April 2016.

(iv) Suman Samui, Indrajit Chakrabarti and Soumya K. Ghosh, "An Improved Single Channel Phase-Aware Speech Enhancement Technique for Low SNR Signal", accepted on 8th March, 2016 for publication in *IET Signal Processing*, DOI: 10.1049/iet-spr.2015.0182.

(v) P.P. Shiju, Indrajit Chakrabarti, Rishi Virdi and Harsh Kaushik, "VLSI Architecture for Block-Matching Motion Estimation Using Adaptive Rood Pattern Search Algorithm", accepted on 10th December, 2015 for publication in *IET Circuits, Devices and Systems*.

(vi) N. Prasad, S. Chattopadhyay and I. Chakrabarti, “Reconfigurable data parallel constant geometry fast Fourier transform architectures on Network-on-Chip”, *Elsevier Microprocessors and Microsystems*, vol. 39, issue 8, November 2015, pp. 741-751.

(vii) B.K.N. Srinivasa Rao, I. Chakrabarti and M. Nawaz Ahmad, “High-speed low-power very -large-scale integration architecture for dual-standard deblocking filter", *IET Circuits, Devices and Systems*, vol. 9, issue 5, pp. 377-383, September 2015, doi:10.1049/iet-cds.2014.0310, Print ISSN 1751-858X, Online ISSN 1751-8598.

(viii) D. Bera, I. Chakrabarti and S.S. Pathak, “Modelling of Cooperative Spectrum Sensing over Rayleigh Fading without CSI in Cognitive Radio Networks”, *Springer Journal on Wireless Personal Communication (WPC)*, Digital Object Identifier: 10.1007/s11277-015-2988-8, published online: 31 July 2015, vol. 86, no. 3, pp. 1281-1297, March 2016.

(ix) M. Panigrahy, I. Chakrabarti and A.S. Dhar, “Low-Delay Parallel Architecture for Fractal Image Compression”, *Springer Circuits Systems and Signal Processing* (ISSN 0278-081X), DOI 10.1007/s00034-015-0088-3, vol. 35, no. 3, pp. 897-917, published online: 04 June 2015.

(x) I. Hatai, I. Chakrabarti and S. Banerjee, “An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multistandard DUC”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 6, June 2015, pp. 1150-1154.

(xi) I. Hatai, I. Chakrabarti and S. Banerjee, “An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Algorithm for Reconfigurable FIR Filter Synthesis”, *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 62, no. 4, April 2015, pp. 1071-1080.

(xii) B.Biswas, R.Mukherjee and I.Chakrabarti, "Efficient architecture of adaptive rood pattern search technique for fast motion estimation", *Elsevier Microprocessors and Microsystems*, Vol. 39, issue 3, May 2015, pp. 200-209, digital object identifier:10.1016/j.micpro.2015.02.004. Published online 24 February 2015. [ No of Pages = 10]

(xiii) B. Biswas, R. Mukherjee, P. Saha and I.Chakrabarti, "An Efficient VLSI Architecture for the Enhanced Three Step Search Algorithm", Springer Journal of The Institution of Engineers (India): series B, digital object identifier: **10.1007/s40031-014-0177-x. Published online 20 February 2015. [No. of pages = 7]**

(xiv) R. Mukherjee, K. Sheth, A.S. Dhar, I. Chakrabarti and S. Sengupta, “High Performance VLSI Architecture for Three Step Search Algorithm”, *Springer Circuits, Systems and Signal Processing*, vol. 34, issue 5, pp. 1595-1612, May 2015, Digital Object Identifier: 10.1007/s00034-014-9919-x, published online: 14 November 2014 [Impact factor 1.26]

(xv) S.M. Karim and I. Chakrabarti, "High Throughput Turbo Decoder Using Pipelined Parallel Architecture and Collision Free Interleaver", *IET Communications*, vol. 6, no. 11, pp. 1416-1424, July 2012.

(xvi) S. M. Karim, G. Mahale and I. Chakrabarti, "A Pipelined Architecture for High Throughput Efficient Turbo Decoder", International Journal of Computer Applications (0975-8887) Special Issue on Electronics, Information and Communication Engineering, Foundation of Computer Science, USA, vol. ICEICE, no. 1, pp 12-16, December 2011.

(xvii) I. Hatai and I. Chakrabarti, "A New High-Performance Digital FM Modulator and Demodulator for Software-Defined Radio and Its FPGA Implementation", International Journal of Reconfigurable Computing, Hindawi Publishing Corporation, Volume 2011 (2011), Article ID 342532, 10 pages, doi:10.1155/2011/342532, Received 31 March 2011; Accepted 8 September 2011.

(xviii) Sumit K. Chatterjee and I. Chakrabarti, "Power Efficient Motion Estimation Algorithm and Architecture Based On Pixel Truncation", *IEEE Transactions on Consumer Electronics*, vol. 57, no. 4, pp. 1782-1790, November 2011.

(xix) I. Hatai and I. Chakrabarti, "Programmable Common Baseband Modulator for Software Defined Radio Systems", *International Journal of Signal and Imaging Systems Engineering (IJSISE)*, InderScience Publishers, vol. 4, no. 3, pp. 142-152, 2011.

(xx) Sumit K. Chatterjee and I. Chakrabarti, "A Fast and Low Power VLSI Architecture for Half-Pixel Motion Estimation Using Two-step Search Algorithm, *IETE Journal of Research*, vol. 57, no. 3, pp. 263-270, 2011.

(xxi) I. Hatai and I. Chakrabarti, "A High-Speed Low-Power Low-Latency Pipelined ROM-less DDFS", *Communications in Computer and Information Science*, Springer DOI:10.1007/978-3-642-17881-8-11, vol. 133, part 2, pp. 108-119, January 2011.

(xxii) Sumit K. Chatterjee and I. Chakrabarti, "Low Power VLSI Architectures for One Bit Transformation based Fast Motion Estimation", *IEEE Transactions on Consumer Electronics*, vol. 56, no. 4, pp. 2652-2660, November 2010.

(xxiii) I. Hatai and I. Chakrabarti, "Multi-Standard Programmable Baseband Modulator for Next Generation Wireless Communications", *International Journal of Computer Networks and Communications (IJCNC)*, Academy & Industry Research Collaboration Center (AIRCC), vol. 2, no. 4, pp. 58-71, July 2010, DOI:10.5121/ijcnc.2010.2406

(xxiv) S.M. Karim and I. Chakrabarti, "An Improved Low-Power High-Througput Log-MAP Turbo Decoder", *IEEE Transactions on Consumer Electronics*, vol. 56, no. 2, pp. 450-457, May 2010.

(xxv) K. Goswami, I. Chakrabarti and S. Sural, "A Probabilistic Adaptive Algorithm for Constructing Hierarchical Meshes", *IEEE Transactions on Consumer Electronics*, vol. 55, no. 3, pp. 1690-1698, August 2009.

(xxvi) C. Rambabu and I. Chakrabarti, "An Efficient Hillclimbing-based Watershed Algorithm and its Prototype Hardware Architecture", *Journal of*

*Signal Processing Systems*, Springer New York, ISSN 1939-8018, DOI: 10.1007/s11265-007-0157-3, vol. 52, no. 3, pp. 281-295, January 2008.

(xxvii) C. Rambabu and I. Chakrabarti, "An Efficient Immersion-based Watershed Transform Method and its Prototype Architecture", *Journal of Systems Architecture*, Elsevier, ISSN 1383-7621, Vol. 53, No. 4, pp. 210-226, April 2007.

(xxviii) C. Rambabu, I. Chakrabarti and A. Mahanta, "Flooding-based watershed algorithm and its prototype hardware architecture" *IEE Proceedings — Vision, Image and Signal Processing*, Vol. 151, No. 3, pp. 224-234, June 2004.

(xxix) P.R. Rao and I. Chakrabarti, "High-performance compensation technique for the radix-4 CORDIC algorithm" in *IEE Proceedings—Computers and Digital Techniques*, Vol. 149 No. 5, September 2002, pp. 219-228.

(xxx) P.N. Swamy, I. Chakrabarti and D. Ghosh, "Architecture for motion estimation using the onedimensional hierarchical search block-matching algorithm" in *IEE Proceedings — Computers and Digital Techniques*, Vol. 149 No. 5, September 2002, pp. 229-239.

(xxxi) I. Chakrabarti, D. Sarkar and A.K. Majumdar, "Identification of Inductive Properties During Verification of Synchronous Sequential Circuits" in *Journal of Automated Reasoning, Kluwer Academic Publishers* , Vol. 14 No. 3, June 1995, pp. 427-462.

**2. Publications in conference proceedings (1994 till date):**

(i) Sandip Das, Suvra Sekhar Das and Indrajit Chakrabarti, "Hardware Implementation of MIMO OFDMA Test Bed and its Application towards Channel Characterization on Indoor Lab Test Environment", accepted and presented in 22$^{nd}$ *National Conference on Communications (NCC-2016)*, 4$^{th}$-6$^{th}$ March, 2016, IIT Guwahati, India.

(ii) Noor-e-Karishma Shaik, B.K.N. Srinivasa Rao and I ndrajit Chakrabarti, "Compressive Sensing based Scalable Video Coding for Space Applications", accepted and presented in 22nd National Conference on Communications (NCC-2016), 4th-6th March, 2016, IIT Guwahati, India.

(iii) Mamata Panigrahy, Indrajit Chakrabarti and Anindya S. Dhar, "Hardware Implementation of Quadtree based Fractal Image Decoder", accepted and presented in 22nd National Conference on Communications (NCC-2016), 4th-6th March, 2016, IIT Guwahati, India.

(iv) Radhika V. Menon, Poulami Raha and Indrajit Chakrabarti, "Classification of Breast Mass in Ultrasound Images using CAD: A Survey", accepted and presented in *International Conference on Systems in Medicine and Biology (ICSMB)*, 4-6 January 2016, IIT Kharagpur India.

(v) N Prasad, Santanu Chattopadhyay, and Indrajit Chakrabarti, "ZMesh: An Energy-Efficient Network-on-Chip Topology for Constant-Geometry Algorithms," in *IEEE International Symposium on Nanoelectronic and Information Systems*, 21-23 Dec. 2015, Radisson BLU Hotel, Indore, India.

(vi) Radhika V. Menon, Poulami Raha, Shweta Kothari, Sumit Chakraborty, Indrajit Chakrabarti and Rezaul Karim, "Automated Detection and Classification of Mass from Breast Ultrasound Images", accepted in *Fifth National Conference on Computer Vision, Pattern Recognition, Image Processing and Graphics (NCVPRIPG)*, 16-19 December, 2015, IIT Patna, India.

(vii) Subhomoy Bhattacharyya, Indrajit Chakrabarti, Maheshkumar H. Kolekar , "Complexity Assisted Consistent Quality Rate Control for High Resolution H.264 Video Conferencing", accepted in The Fifth National Conference on Computer Vision, Pattern Recognition, Image Processing and Graphics (NCVPRIPG), 16-19 December, 2015, IIT Patna, India.

(viii) Sandip Das, Indrajit Chakrabarti and Suvra Sekhar Das, "Hardware implementation of Frequency Domain Link Adaptation for OFDMA based Systems", accepted and presented in 21st National Conference on Communications (NCC-2015), 27th Feb – 1st March, 2015, IIT Bombay, India, DOI: 10.1109/NCC.2015.7084895.

(ix) R. Mukherjee, B. Biswas and I. Chakrabarti, "Efficient FPGA-based design of hexagonal search algorithm for motion estimation", accepted for presentation in *Real-Time Image and Video Processing 2015 Conference* (part of IS&T/SPIE Electronic Imaging 2015 Conference), 8-12 Feb, 2015, San Francisco, California, USA.

(x) R. Mukherjee, B. Biswas and I. Chakrabarti, "An Efficient VLSI Architecture for Motion Estimation using New Three Step Search Algorithm", accepted for presentation in *TENCON 2014 conference*, 22-25 October, 2014, Bangkok, Thailand.

(xi) N. Prasad, S. Chattopadhyay and I. Chakrabarti, "NoC Based Multiplier-less Constant Geometry FFT Architecture", presented and published in proceedings of 4th *International Conference on Emerging Applications of Information Technology* (EAIT-2014), 19-21 Dec, 2014, Indian Statistical Institute, Kolkata, India.

(xii) M. Panigrahy, I. Chakrabarti and A.S. Dhar, "VLSI Design of Fast Fractal Image Encoder", accepted and presented in *18th International Symposium on VLSI Design (VDAT-2014)*, 16-18 July 2014, PSG College of Technology, Coimbatore, India.

(xiii) D. Bera, I. Chakrabarti and S.S. Pathak, "Cooperative Spectrum Sensing over Correlated Rayleigh Fading Channels in Cognitive Radio using Factor

Graph", accepted and presented in *IEEE International Conference on Communications (ICC-2014),* 10-14 June 2014, Sydney, Australia.

(xiv) D. Bera, S. Maheswari, I. Chakrabarti and S.S. Pathak, "Decentralized Cooperative Spectrum Sensing in Cognitive Radio without Fusion Centre", accepted and presented in *20th National Conference on Communications (NCC-2014),* Feb 28-March 2, 2014, IIT Kanpur, India.

(xv) R. Mukherjee, I. Chakrabarti and S. Sengupta, "FPGA Based Implementation of Intra-Prediction Based Encoding of H.264", *accepted for presentation in International Conference on VLSI and Signal Processing (ICVSP-2014),* Dec 10-12, 2014, IIT Kharagpur, India.

(xvi) B.K.N. Srinivasarao, A. Mondal and I. Chakrabarti, "FPGA implementation of In-Band Motion Compensated Temporal Filtering for scalable Video coding", *accepted for presentation in International Conference on VLSI and Signal Processing (ICVSP-2014),* Dec 10-12, 2014, IIT Kharagpur, India.

(xvii) M. Panigrahy, I. Chakrabarti and A.S. Dhar, "Architecture for Fractal Image Encoder", *accepted for presentation in International Conference on VLSI and Signal Processing (ICVSP-2014),* Dec 10-12, 2014, IIT Kharagpur, India.

(xviii) P.P. Shiju, R.K. Pillai and I. Chakrabarti, "Low Power VLSI Architecture for 2D Active Mesh Based Motion Estimation, *accepted for presentation in International Conference on VLSI and Signal Processing (ICVSP-2014),* Dec 10-12, 2014, IIT Kharagpur, India.

(xix) I. Hatai, I. Chakrabarti and S. Banerjee, "FPGA Implementation of a Fetal Heart Rate Measuring System", *accepted for presentation in 2nd International Conference on Advances in Electrical Engineering (ICAEE-2013),* Dec 19-21, 2013, Dhaka, Bangladesh.

(xx) R. Mukherjee**,** V. Mahajan, I. Chakrabarti, and S. Sengupta, "High Performance VLSI Implementation of Context-based Adaptive Variable Length Coding (CAVLC) for H.264 Encoder", *accepted for presentation in 2013 National Conference on Computer Vision, Pattern Recognition, Image Processing and Graphics (NCVPRIPG),* Dec 18-21, 2013, IIT-Rajasthan (Jodhpur), India.

(xxi) Sumit K. Chatterjee and I. Chakrabarti, "Algorithm and Architecture for Quarter Pixel Motion Estimation for H.264/AVC", *accepted for presentation in 2013 National Conference on Computer Vision, Pattern Recognition, Image Processing and Graphics (NCVPRIPG),* Dec 18-21, 2013, IIT-Rajasthan (Jodhpur), India.

(xxii) R. Mukherjee**,** E. Sandeep, I. Chakrabarti, and S. Sengupta, "VLSI Architecture of Forward and Inverse Quantization Modules of H.264 for HD Transmission", *Proceedings of INDICON 2013,* Dec 13-15, 2013, IIT-Bombay, Mumbai, India.

(xxiii) R. Mukherjee**,** V. Mahajan, I. Chakrabarti, and S. Sengupta, "High Performance VLSI Implementation of CAVLC Decoder of H.264/AVC for

HD Transmission", *Proceedings of INDICON 2013*, Dec 13-15, 2013, IIT-Bombay, Mumbai, India.

(xxiv) R. Mukherjee**,** S. Keyur, E. Sandeep, I. Chakrabarti, S. Sengupta, "FPGA Based VLSI Implementation of Quantization and its Inverse for H.264 Codec", *Proceedings of 2013 IEEE Conference on Information and Communication Technologies (ICT)*, 11-12 April 2013, Thuckalay, Tamil Nadu, India.

(xxv) D. Bera, I. Chakrabarti, P. Ray and S.S. Pathak, "Factor Graph based Cooperative Spectrum Sensing in Cognitive radio over Time Varying Channels", *Proceedings of IEEE 77$^{th}$ Vehicular Technology Conference (VTC-2013 Spring)*, June 2-5, 2013, Dresden, Germany.

(xxvi) I. Hatai, I. Chakrabarti and S. Banerjee, "Reconfigurable Architecture of a RRC FIR Interpolator for Multi-Standard Digital Up-Convertor", accepted for presentation in *20$^{th}$ Reconfigurable Architectures Workshop (RAW) associated with 27$^{th}$ Annual International Parallel and Distributed Processing Symposium (IPDPS 2013)*, May 20-21, 2013, Boston, USA.

(xxvii) R. Mukherjee, W. Hari Prasad, P. Dheeraj, I. Chakrabarti and S. Sengupta, "FPGA Based Pipelined Implementation of Fast 2-D 4×4 Inverse Transform of H.264", *Proceedings of 7$^{th}$ International Conference on Computer and Electrical Engg (ICECE 2012)*, 20-22 December 2012, Dhaka, Bangladesh.

(xxviii) R. Mukherjee**,** I. Chakrabarti, S. Sengupta, "FPGA Based Architectural Implementation of Context-Based Adaptive Variable Length Coding (CAVLC) for H.264/AVC". *Proceedings of IET International Conference on Information Science and Control Engineering (ICISCE 2012)*, 7-9 December 2012, Shenzhen, China.

(xxix) D. Bera, S.S. Pathak and I. Chakrabarti, "A Normal Factor Graph Approach for Cooperative Spectrum Sensing in Cognitive Radio", *Proceedings of National Conference on Communication* (NCC-2012), pp. 6-10, 3-5 February 2012, IIT Kharagpur, India.

(xxx) R. Mukherjee, W. Hari Prasad, P. Dheeraj, I. Chakrabarti and S. Sengupta, "High Throughput Pipelined Architecture for Fast 2-D 4×4 Forward Integer Transform of H.264", *Proceedings of National Conference on Communication* (NCC-2012), 3-5 February 2012, IIT Kharagpur, India.

(xxxi) S.M. Karim and I. Chakrabarti, "Design of Efficient High Throughput Pipelined Parallel Turbo Decoder using QPP Interleaver", *Proceedings of International* Conference *on Multimedia, Signal Processing and Communication Technologies* (IMPACT-2011), pp. 248-251, 17-19 December, 2011, AMU, Aligarh, India.

(xxxii) D. Bera, S.S. Pathak and I. Chakrabarti, "Factor Graph Based CRSC Turbo Code and Iterative Receiver Design", *Proceedings of IEEE TENCON*, pp. 893-897, November, 2011, Bali, Indonesia.

(xxxiii) S. M. Karim, G. Mahale and I. Chakrabarti, "A Pipelined Architecture for High Throughput Efficient Turbo Decoder", *Proceedings of International Conference on Electronics, Information and Communication Systems Engineering* (ICEICE-2010), 28-30 March 2011, Jodhpur, India.

(xxxiv) I. Hatai and I. Chakrabarti, "Parameter Controlled Reconfigurable Baseband Modulator for SDR Architecture", *Proceedings of 2nd International Conference on Mechanical and Electronic Engineering* (ICMEE 2010), 1-3 August, 2010, Kyoto, Japan.

(xxxv) I. Hatai and I. Chakrabarti, "Reconfigurable Digital FM Modem for SDR Application", *Proceedings of International Conference on "Recent Advancements in Electrical Sciences* (ICRAES'10), 8-9 January 2010, Chennai, India

(xxxvi) I. Hatai and I. Chakrabarti, "Design and Implementation of a Programmable Baseband Modulator for SDR Architecture", *Proceedings of First International conference on VLSI Design & Communication Systems* (ICVLSICOM-10), 8-10 January 2010, Chennai, India

(xxxvii) I. Hatai and I. Chakrabarti, "Digital FM Modem for SDR Architecture", *Proceedings of 4th International Conference on Computers and Devices for Communication* (CODEC-09) , Kolkata, India 14-16 December 2009

(xxxviii) I. Hatai, and I Chakrabarti, "FPGA Implementation of a High Performance Digital FM Demodulator", *Proceedings of International Conference on Modelling and Simulation*, Trivandrum, Kerala, India 1-3 December 2009

(xxxix) I. Hatai and I. Chakrabarti, "FPGA Implementation of a Digital FM Modem", *Proceedings of ICIMT-2009 (International Conference on Information and Multimedia Technology)* published by IEEE Computer Society CPS (Conference Publishing Services), pp. 475-479, Jeju Island, South Korea, Dec. 16-18, 2009.

(xl) J. Gurugubelli, I. Chakrabarti and S. Chakrabarti, "Design and implementation of a generalized parameterizable modulator for a reconfigurable radio" *Proceedings of TENCON 2009*, Singapore, 23-26 November, 2009.

(xli) S. K. Chatterjee and I. Chakrabarti, "A High Performance VLSI Architecture for Fast Two-Step Search Algorithm for Sub-Pixel Motion Estimation", *Proceedings of IMPACT-2009 (International Conference on Multimedia, Signal Processing and Communication Technologies)*, pp. AMU, Aligarh, AMU, Aligarh, India, Mar. 14-16, 2009.

(xlii) B. Mohanarao and I. Chakrabarti, "An Efficient Low-Power VLSI Architecture for Four Step Search Algorithm", *Proceedings of ICCVGIVP-2009 (Indian Conference on Comp. Vision, Graphics, Image and Video Proc.)*, pp. 127-131, SRKNE College, Nagpur, India, Mar. 13-14, 2009.

(xliii) K. Goswami, S. Sural and I. Chakrabarti, "A Probabilistic Algorithm for Constructing Hierarchical Mesh in Video Encoders", *Proceedings of ICCVGIVP-2009 (Indian Conference on Comp. Vision, Graphics, Image and Video Proc.)*, pp. 104-107, SRKNE College, Nagpur, India, Mar. 13-14, 2009.

(xliv) B.K.N. Srinivasarao and I. Chakrabarti, "A Parallel Architecture for Successive Elimination Block Matching Algorithm", *Proceedings of ICVGIP-2008 (6th Indian Conference on Comp. Vision, Graphics and Image Proc.)*, pp. 226-231, Bhubaneswar, India, Dec. 16-19, 2008.

(xlv) T. Suman, S.K. Chatterjee and I. Chakrabarti, "High Speed and Memory Efficient Parallel Bit Plane Coding Architecture for JPEG2000", *Proceedings of ICVGIP-2008 (6th Indian Conference on Comp. Vision, Graphics and Image Proc.)*, pp. 232-237, Bhubaneswar, India, Dec. 16-19, 2008.

(xlvi) S.K. Chatterjee and I. Chakrabarti, "A Memory Efficient Architecture for Diamond Search Block Matching Algorithm", *Proceedings of ICACT-2008 (International Conference on Advanced Computing Technologies)*, pp. 53-59, Hyderabad, India, Dec. 26-27, 2008.

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**Thesis Guidance:**

Ph.D. (completed): (i) C. Rambabu (degree awarded in 2006); title : "Efficient Watershed Algorithms for Image Segmentation and Related Prototype Architectures" (ii) J. Bhaumik (co-guided with Prof. D. Roychowdhury of Dept. of Compute Science & Engg., IIT Kharagpur) (degree awarded in 2011); title: "Design and Implementation of Error Correcting Codes and Cryptographic Primitives"

(iii) S. K. Chatterjee (degree awarded in 2011); title: "Low Power Motion Estimation Algorithms and Architectures for Efficient Video Compression" (iv) S.M. Karim (degree awarded in 2013); title: "VLSI Architecture for High Throughput Turbo Decoder and Reduced Complexity Turbo Equalizer"

M.S. (completed) : (i) I. Hatai, (ii) K. Goswami (co-guided with Prof. S. Sural of School of Information Technology, IIT Kharagpur), (iii) Subhomoy Bhattacharyya (co-guided with Prof. A. Bhattacharyya of Dept. of Electronics & ECE, IIT Kharagpur)

No. of M. Tech. thesis guided (2006 till date): 16
No. of B. Tech. thesis guided (2005 till date): 16

**Short-term courses (STCs) organized / delivered lectures (2006 till date)**

Following lectures were delivered :-

(i) "Video Compression Architectures" in AICTE Summer School on "TCAD for VLSI Design", June 1-6, 2009, Andhra University Engg. College, Visakhapatnam

(ii) "VLSI Testing" in AICTE Summer School on "TCAD for VLSI Design", June 1-6, 2009, Andhra University Engg. College, Visakhapatnam

(iii) "Field Programmable Gate Array (FPGA)" in Short Term Course on "Embedded System Design", Feb. 2-6, 2009, IIT Kharagpur.

(iv) "VLSI Testing" in AICTE Winter School on "TCAD for VLSI Design", Dec 15-22, 2008, IIT Kharagpur extension centre in Bhubaneswar

(v) "Video Compression Architectures" in AICTE Winter School on "TCAD for VLSI Design", Dec 15-22, 2008, IIT Kharagpur extension centre in Bhubaneswar

(vi) "VLSI Testing" in AICTE Summer School on "TCAD for VLSI Design", June-July, 2008, IIT Kharagpur

(vii) "Video Compression Architectures" in AICTE Summer School on "TCAD for VLSI Design", June-July, 2008, IIT Kharagpur

(viii) "DCT and Motion Compensation Architectures" in AICTE Summer School on "Image and Video Processing", June 30 – July 11, 2008, IIT Kharagpur

(ix) "Java Applet Programming" in Summer School on "C++ and Java", June 2007, IIT Kharagpur

(x) "DSP Microprocessor Architectures" in IEP (Instruction Enhancement Programme) on VLSI DSP, Sep 24 – Oct 5, 2007, IIT Kharagpur

(xi) "High Performance VLSI Architectures" in IEP (Instruction Enhancement Programme) on VLSI DSP, Sep 24 – Oct 5, 2007, IIT Kharagpur

(xii) "Verilog Hardware Description Language" in IEP (Instruction Enhancement Programme) on VLSI DSP, Sep 24 – Oct 5, 2007, IIT Kharagpur

(xiii) "ADSP-2181 DSP Processor", in STC on "DSP Tools and Practice", June 04-09, 2007, IIT Kharagpur

(xiv) "DSP Architectures" in STC on "Embedded Systems and Technology", June 25-30, 2007, IIT Kharagpur

(xv) "VLSI Architectures for Video Compression" in STC on "Image and Video Processing", Feb 19 – March 2, 2007

(xvi) "VLSI Architectures for Low-Power Signal Processing" in IEP on Low-Power VLSI Design, Sep 11-22, 2006, IIT Kharagpur

(xvii) "DSP Architectures" in STC on "Embedded Systems and Technology", June 19-24, 2006, IIT Kharagpur