Rajat Subhra Chakraborty

Professor
Department of Computer Science and Engineering
Indian Institute of Technology Kharagpur
Kharagpur, West Bengal, INDIA 721302

E-mail: rschakraborty@cse.iitkgp.ac.in
rschakraborty@gmail.com

Website: http://cse.iitkgp.ac.in/~rschakraborty
Google Scholar Profile: https://scholar.google.co.in/citations?user=ITIg9kkAAAAJ&hl=en
Scopus Profile: https://www.scopus.com/authid/detail.uri?authorId=56194286800
Linkedin Profile: https://in.linkedin.com/in/rajat-subhra-chakraborty-9249709

Phone (IIT office): +91 3222 281792
Fax (IIT CSE Department): +91 3222 255303

EDUCATION

- **Ph.D.** in Computer Engineering, Department of Electrical Engineering and Computer Science, Case Western Reserve University, Cleveland, Ohio, USA.
  Duration: Aug. 2006 - May 2010
  Advisor: Prof. Swarup Bhunia
  Dissertation: **Hardware Security through Design Obfuscation**
  CGPA: 4.00/4.00
- **B.E. (Honors)** in Electronics and Telecommunication Engineering, Jadavpur University, Kolkata, India.
  Duration: 2001 - 2005
  CGPA: 3.84/4.00

PROFESSIONAL EXPERIENCE

- **Professor,** *Dept. of Computer Science and Engineering*, Indian Institute of Technology Kharagpur, Kharagpur, West Bengal, India (Mar. 2023- present)
- **Offensive Security Researcher,** Intel Corporation, Bangalore, India [on leave from IIT Kharagpur], (Dec. 2021- Feb. 2023)
- **Associate Professor,** *Dept. of Computer Science and Engineering*, Indian Institute of Technology Kharagpur, Kharagpur, West Bengal, India (Feb. 2016 - present)
- **Assistant Professor,** *Dept. of Computer Science and Engineering*, Indian Institute of Technology Kharagpur, Kharagpur, West Bengal, India (Jun. 2010 – Feb. 2016)
- **Engineering Co-op**, *Advanced Micro Devices* (AMD), Sunnyvale, CA, USA **(**Sep. 2007-Dec. 2007**).**
- **CAD Software Engineer,** *National Semiconductor*, Bangalore, India **(**Jul. 2005-Jul. 2006)
- **Engineering Co-op,** *National Semiconductor*, Bangalore, India **(**Jun. 2004-Aug. 2004)

RESEARCH AND PUBLICATIONS

- **Research Interests:**
  - Hardware Security and Applied Cryptography
  - VLSI
  - Digital Content Protection
  - Digital Image Forensics

- **Edited Volume**
  1. S. Roy, **R. S. Chakraborty**, J. Mathew, A. P Mazumdar and S. Chakraborty (eds.) "Artificial Intelligence and Deep Learning for Computer Network: Management and Analysis", *CRC Press* (forthcoming).
  2. **R. S. Chakraborty**, J. Mathew and A. V. Vasilakos (eds.), "Security and Fault Tolerance in Internet of Things", *Springer* (ISBN: 9783030028060 print, ISBN: 9783030028077 e-book).
  3. **R. S. Chakraborty**, P. Schwabe and J. Solworth (eds.), "Proceedings of the 5th International Conference on Security, Privacy and Applied Cryptography Engineering (SPACE) 2015", *Lecture Notes in Computer Science* vol. 9354, *Springer*.
  4. **R. S. Chakraborty**, V. Matyas and P. Schaumont (eds.), "Proceedings of the 4th International Conference on Security, Privacy and Applied Cryptography Engineering (SPACE) 2014", *Lecture Notes in Computer Science* vol. 8804, *Springer*.

- **Books**
  1. P. Santikellur and **R. S. Chakraborty**, "Deep Learning for Computational Problems in Hardware Security: Modeling Attacks on Strong Physically Unclonable Function Circuits", *Springer* (ISBN: 9789811940163 print, 978-981-19-4017-0 e-book).
  2. A. Roy, R. Dixit. R. Naskar and **R. S. Chakraborty**, "Digital Image Forensics - Theory and Implementation", *Springer* (ISBN: 9789811076435 print, 9789811076442 e-book).
  3. A. Palchaudhuri and **R. S. Chakraborty**, "High Performance Integer Arithmetic Circuit Design on FPGA: Architecture, Implementation and Design Automation", *Springer* (ISBN: 9788132225195 print, 9788132225201 e-book).
  4. D. Mukhopadhyay and **R. S. Chakraborty**, "Hardware Security: Design, Threats and Safeguards", *CRC Press* (USA) (ISBN: 9781439895832).
  5. R. Naskar and **R. S. Chakraborty**, "Reversible Digital Watermarking: Theory and Practices", *Morgan Claypool* (USA), (ISBN: 9781627053150 print, ISBN: 9781627053167 e-book).

- **Book Chapters**
  1. P. Santikellur, **R. S. Chakraborty** and S. Bhunia, "Hardware IP Protection Using Register Transfer Level Locking and Obfuscation of Control and Data Flow" in S. Katkoori and S. A. Islam (eds.), "Behavioral Synthesis for Hardware Security", *Springer*, 2022 (ISBN 978-3-030-78840-7 print, ISBN 978-3-030-78841-4 (eBook)).
  2. S. R. Rajendran and **R. S. Chakraborty**, "Online Checkers to Detect Hardware Trojans in AES Hardware Accelerators", in S. Saini, K. Lata and G. R. Sinha (eds.), "VLSI and Hardware Implementations Using Modern Machine Learning Methods", *CRC Press*, 2022 (ISBN: 9781003201038).

3. **R. S. Chakraborty** and R. Mukherjee, “FPGA Security (invited chapter)”, in S. Sajodia, P. Samarati and M. Yung (eds.), “Encyclopedia of Cryptography, Security and Privacy”, *Springer*, 2019 (ISBN: 9783642277399).
4. P. Santikelllur, **R. S. Chakraborty** and J. Mathew, “Hardware Security in the Context of Internet of Things: Challenges and Opportunities”, in U. Ghosh, D. B. Rawat, R. Datta and A. K. Pathan (eds.), “Internet of Things and Secure Smart Environments: Success and Pitfalls”, *CRC Press*, 2020 (ISBN: 9780367276706).
5. V. Govindan and **R. S. Chakraborty**, "Logic Testing for Hardware Trojan Detection", in S. Bhunia and M. Tehranipoor (eds.), "The Hardware Trojan War: Attacks, Myths, and Defenses", *Springer*, 2017 (ISBN: 9783319685106).
6. **R. S. Chakraborty** and S. Bhunia, “State Space Obfuscation and its Applications in Hardware Security”, in D. Forte, S. Bhunia and M. Tehranipoor (eds.), “Hardware Protection through Obfuscation”, *Springer*, 2017 (ISBN: 9783319490199).
7. R. Naskar, P. Malaviya and **R. S. Chakraborty**, “Digital Forensics: State-of-the-Art and Open Problems”, in R. Pal (ed.), “Innovative Research in Attention Modeling for Computer Vision Applications”, *IGI Global*, 2015 (ISBN: 9781466687233 print, ISBN: 9781466687240 e-book).
8. A. Palchaudhuri and **R. S. Chakraborty**, “A Fabric Component based Approach to the Architecture and Design Automation of High Performance Integer Arithmetic Circuits on FPGA”, in M. Fakhfakh, E. Tlelo-Cuautle and P. Siarry (eds.), “Computational Intelligence in Analog and Mixed-Signal (AMS) and Radio-Frequency (RF) Circuit Design”, *Springer*, 2015 (ISBN: 9783319198712 print, ISBN: 9783319198729 e-book).
9. **R. S. Chakraborty**, S. Bhunia and Y. Zheng, “RTL IP Protection and Secure SoC Design: a Design Obfuscation based Approach”, in C. H. Chang and M. Potkonjak (eds.), “Secure System Design and Trustable Computing”, Springer, 2015 (ISBN: 9783319149707 print, ISBN: 9783319149714 e-book).
10. R. Naskar and **R. S. Chakraborty**, “Reversible Watermarking: Theory and Practice”, in B. Issac (ed.), “Case Studies in Secure Computing – Achievements and Trends”, *CRC Press*, 2014 (ISBN: 9781482207064 print, ISBN: 9781482207071 e-book).
11. R. Naskar, **R. S. Chakraborty**, D. K. Das and C. Chakraborty, “Digital Image Watermarking: Impact on Medical Imaging Applications in Telemedicine”, in Dr. R. Srivastava (ed.), “Recent Advances in Computer Vision and Image Processing: Methodologies and Applications”, *IGI Global*, 2013 (ISBN 9781466645585).

- **Journal Papers** (in reverse chronological order)
  1. R. Mukherjee and **R. S. Chakraborty**, “Attacks on Recent DNN IP Protection Techniques and Their Mitigation”, accepted in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.*
  2. D. Das, R. Naskar and **R. S. Chakraborty**, "Image Splicing Detection with Principal Component Analysis Generated Low-dimensional Homogeneous Feature Set based on Local Binary Pattern and Support Vector Machine", accepted in *Multimedia Tools and Applications* (Springer), 2023.
  3. K. Pratihar, U. Chatterjee, M. Alam, D. Mukhopadhyay, and **R. S. Chakraborty**, "Birds of the Same Feather Flock Together: A Dual-Mode Circuit Candidate for Strong PUF-TRNG Functionalities", accepted in *IEEE Transactions on Computers*.

4. D. Singh, P. Singh, R. Jena and **R. S. Chakraborty**, “An Image Forensic Technique Based on JPEG Ghosts”, *Multimedia Tools and Applications* (Springer), vol. 82, no. 9, pp. 14153-14169, Apr. 2023.
5. P. Santikellur, M. Buddhanoy, S. Sakib, B. Ray and **R. S. Chakraborty**, “A Shared Page-Aware Machine Learning Assisted Method for Predicting and Improving Multi-Level Cell NAND Flash Memory Life Expectancy”, *Microelectronics Reliability* (Elsevier), 2023, vol. 140, pp. 114867, Jan. 2023.
6. P. Santikellur and **R. S. Chakraborty**, “Correlation Integral based Intrinsic Dimension: a Deep Learning Assisted Empirical Metric to Estimate the Robustness of Physically Unclonable Functions to Modeling Attacks”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 4, pp. 3216-3227, Oct. 2022.
7. R. Mukherjee, S. R. Rajendran and **R. S. Chakraborty**, "A Comprehensive Survey of Physical and Logic Testing Techniques for Hardware Trojan Detection and Prevention", *Journal of Cryptographic Engineering* (Springer), vol. 12, no. 4, pp. 495-522, Nov. 2022. Note: This is an extended version of the paper published in ACM International Workshop on Attacks and Solutions in Hardware Security (ASHES), [post-conference workshop co-located with ACM CCS], Virtual Workshop, Nov. 2020.
8. R. Mukherjee and **R. S. Chakraborty**, “Novel Hardware Trojan Attack on Activation Parameters of FPGA-based DNN Accelerators”, *IEEE Embedded Systems Letters*, vol. 14, no. 3, pp. 131-134, Sep. 2022.
9. M. H. Mahalat, S. Mandal, A. Mondal, B. Sen and **R. S. Chakraborty**, “Implementation, Characterization and Application of Path Changing Switch based Arbiter PUF on FPGA as a lightweight Security Primitive for IoT”, *ACM Transactions on Design Automation of Electronic Systems*, vol. 27, no. 3, pp. 26:1-26:26, May 2022.
10. A. Saha, H. Banerjee, **R. S. Chakraborty** and D. Mukhopadhyay, “ORACALL: An Oracle-Based Attack on Cellular Automata Guided Logic Locking”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 12, pp. 2445-2454, Dec. 2021.
11. S. Chattopadhyay, P. Santikellur, **R. S. Chakraborty**, J. Mathew and M. Ottavi, “A Conditionally Chaotic Physically Unclonable Function Design Framework with High Reliability”, *ACM Transactions on Design Automation of Electronic Systems*, vol. 26, no. 6, pp. 41:1-41:24, Nov. 2021.
12. P. Santikellur and **R. S. Chakraborty**, “A Computationally Efficient Tensor Regression Network based Modeling Attack on XOR Arbiter PUF and its Variants”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 6, pp. 1197-1106, Jun. 2021.
13. R. Mukherjee, V. Govindan, S. Koteshwara, A. Das, K. K. Parhi and **R. S. Chakraborty**, “Probabilistic Hardware Trojan Attacks on Multiple Levels of Reconfigurable Network Infrastructure”, *Journal of Hardware and Systems Security* (Springer), vol. 4, no. 4, pp. 343-360, Dec. 2020.
14. A. Chakraborty, V. Maurya, S. Prasad, S. Gupta, **R. S. Chakraborty** and H. Rahaman, “BDD-based Synthesis Technique for improved mapping of Boolean functions inside Memristive crossbar-slices”, *IET Computers and Digital Techniques*, vol. 15, no. 4, pp. 112-124, Dec. 2020.
15. U. Chatterjee, D. Mukhopadhyay and **R. S. Chakraborty**, “3PAA: A Private PUF Protocol for Anonymous Authentication”, *IEEE Transactions on Information Forensics and Security*, vol. 16, pp. 756-769, Sep. 2020.
16. A. Roy and **R. S. Chakraborty**, “Towards Optimal Prediction Error Expansion based Reversible Image Watermarking”, *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 30, no. 8, pp. 2377-2390, Aug. 2020.

17. U. Chatterjee, S. Chatterjee, D. Mukhopadhyay and **R. S. Chakraborty**, "Machine-Learning Assisted PUF Calibration for Trustworthy Proof of Sensor Data in IoT", *ACM Transactions on Design Automation of Electronic Systems*, vol. 25, no. 4, pp. 32:1-32:21, Jun. 2020.
18. T. Hoque, **R. S. Chakraborty** and S. Bhunia, "Hardware Obfuscation and Logic Locking: a Tutorial Introduction", *IEEE Design & Test*, vol. 37, no. 3, pp. 59-77, Mar. 2020.
19. V. K. Rai, S. Tripathy, **R. S. Chakraborty** and J. Mathew, "HTRNG: High Throughput True Random Number Generator using Memristor", *IEEE VLSI Circuits & Systems Letter* (feature article), vol, 6, no. 1, pp. 1-12, Feb. 2020.
20. P. Ghosh, A. Bhattacharyay, D. Forte and **R. S. Chakraborty**, "Automated Defective Pin Detection for Recycled Microelectronics Identification", *Journal of Hardware and Systems Security* (Springer), vol. 3, no. 3, pp. 250-260, Sep. 2019.
21. D. B. Tariang, **R. S. Chakraborty** and R. Naskar, "A Robust Residual Dense Neural Network for Countering Anti-Forensic Attack on Median Filtered Images", *IEEE Signal Processing Letters*, vol. 26, no. 8, pp. 1132-1136, Aug. 2019.
22. P. Ghosh and **R. S. Chakraborty**, "Recycled and Remarked Counterfeit Integrated Circuit Detection by Image Processing based Package Texture and Indent Analysis", *IEEE Transactions on Industrial Informatics*, vol. 15, no. 4, pp. 1966-1974, Apr. 2019.
23. V. Govindan, **R. S. Chakraborty**, P. Santikellur and A. K. Chaudhary, "A Hardware Trojan Attack on FPGA based Cryptographic Key Generation: Impact and Detection", *Journal of Hardware and Systems Security* (Springer), vol. 2, no. 3, pp. 225-239, Sep. 2018.
24. U. Chatterjee, V. Govindan, R. Sadhukhan, D. Mukhopadhyay, **R. S. Chakraborty**, D. Mahata and M Prabhu, "Building PUF based Authentication and Key Exchange Protocol for IoT without Explicit CRPs in Verifier Database", *IEEE Transactions on Dependable and Secure Computing*, vol. 16, no. 3, May/Jun. 2019, pp. 424-437.
25. D. Basu Roy, M. Alam, S. Bhattacharya, V. Govindan, F. Regazzoni, **R. S. Chakraborty** and D. Mukhopadhyay, "Customized Instructions for Protection Against Memory Integrity Attacks", *IEEE Embedded Systems Letters*, vol. 10, no. 3, pp. 91-94, Sep. 2018.
26. D. P. Sahoo, D. Mukhopadhay, **R. S. Chakraborty** and P. H. Nguyen, "A Multiplexer-Based Arbiter PUF Composition with Enhanced Reliability and Security", *IEEE Transactions on Computers*, vol. 67, no. 3, pp. 403-417, Mar. 2018.
27. Anju P. Johnson, S. Patranabis, **R. S. Chakraborty** and D. Mukhopadhyay, "Remote Dynamic Partial Reconfiguration: A Threat to Internet-of-Things and Embedded Security Applications", *Microprocessors and Microsystems* (Elsevier), vol. 52, no. C, pp. 131-144, Jul. 2017.
28. **R. S. Chakraborty**, Samuel Pagliarini, J. Mathew, Sree Ranjani R. and Nirmala Devi M., "A Flexible Online Checking Technique to Enhance Hardware Trojan Horse Detectability by Reliability Analysis", *IEEE Transaction on Emerging Topics in Computing*, vol. 5, no. 2, pp. 260-270, Jan. 2017.
29. U. Chatterjee, **R. S. Chakraborty** and D. Mukhopadhyay, "A PUF based Secure Communication Protocol for IoT", *ACM Transactions on Embedded Computing Systems*, vol. 16, no. 3, pp. 67:1-67:25, Jul. 2017.
30. **R. S. Chakraborty**, R. R. Jeldi, I. Saha and J. Mathew, "Binary Decision Diagram Assisted Modeling of FPGA-based Physically Unclonable Function by Genetic Programming", *IEEE Transaction on Computers*, vol. 66, no. 6, pp. 971-981, Jun. 2017.
31. P. H. Nguyen, D. P. Sahoo, **R. S. Chakraborty** and D. Mukhopadhyay, "Security Analysis of Arbiter PUF and its Lightweight Compositions under Predictability Tests", *ACM Transactions on Design Automation of Electronic Systems*, vol. 22, no. 2, pp. 20:1-20:28, Feb. 2017.
32. Anju P. Johnson, **R. S. Chakraborty** and D. Mukhopadhyay, "An Improved DCM-based Tunable True Random Number Generator for Xilinx FPGA", *IEEE Transactions on Circuits and Systems-II*, vol. 64, no. 4, pp. 452-456, April 2017.

33. Y. Yang, J. Mathew, **R. S. Chakraborty**, M. Ottavi and D. K. Pradhan, "Low Cost Memristor Associative Memory Design for Full and Partial Matching Applications", *IEEE Transactions on Nanotechnology*, vol. 15, no. 2, pp. 537-538, May 2016.
34. Anju P. Johnson, **R. S. Chakraborty** and D. Mukhopadhyay, "A PUF-enabled Secure Architecture for FPGA-based IoT Applications", *IEEE Transactions on Multi-scale Computing Systems* (special issue on *Wearables, Implants and Internet-of-Things*), vol. 1, no. 2, pp. 110-122, April-June 2015.
35. U. Chatterjee, **R. S. Chakraborty**, H. Kapoor and D. Mukhopadhyay, "Theory and Application of Delay Constraints in Arbiter PUF", *ACM Transactions on Embedded Computing Systems*, vol. 15, no. 1, Feb. 2016, pp. 10:1-10:20.
36. D. P. Sahoo, P. H. Nguyen, D. Mukhopadhyay and **R. S. Chakraborty**, "A Case of Lightweight PUF Constructions: Cryptanalysis and Machine Learning Attacks", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 8, Aug. 2015, pp. 1334 - 1343.
37. J. Mathew, **R. S. Chakraborty**, Y. Yang, D. P. Sahoo and D. Pradhan, "A Novel Memristor based Physically Unclonable Function", *Integration, the VLSI Journal* (*Elsevier*), vol. 51, Sep. 2015, pp. 37-45.
38. R. Naskar and **R. S. Chakraborty**, "A Technique to Evaluate Upper Bounds on Performance of Pixel-Prediction based Reversible Watermarking Algorithms", *Journal of Signal Processing Systems* (*Springer*), vol. 82, no. 3, Mar. 2016, pp. 373-389.
39. J. Mathew, **R. S. Chakraborty**, Y. Yang, D. P. Sahoo and D. Pradhan, "A Novel Memristor based Hardware Security Primitive", *ACM Transactions on Embedded Computing Systems*, vol. 14, no. 3, pp. 60:1-60:20, May 2015.
40. S. Narasimhan, D. Du, **R. S. Chakraborty**, S. Paul, F. Wolff, C. Papachristou, K. Roy and S. Bhunia, "Hardware Trojan Detection by Multiple-Parameter Side-Channel Analysis", *IEEE Transactions on Computers*, vol. 62, no. 11, Nov. 2013, pp. 2183-2195.
41. **R. S. Chakraborty**, I. Saha, A. Palchaudhuri and G. K. Naik, "Hardware Trojan Insertion by Direct Modification of FPGA Configuration Bitstream", *IEEE Design & Test of Computers*, vol. 30, no. 2, Apr. 2013, pp. 45-54 (**most popular article in *IEEE Design & Test of Computers* in the period April-July 2013**).
42. R. Naskar and **R. S. Chakraborty**, "A Generalized Tamper Localization Approach for Reversible Watermarking Algorithms", *ACM Transactions on Multimedia Computing Communications and Applications*, vol. 9, no. 3, Jun. 2013, pp. 19:1-19:22.
43. R. Naskar and **R. S. Chakraborty**, "Histogram–Bin–Shifting based Reversible Watermarking for Color Images", *IET Image Processing*, vol. 7, no. 2, Mar. 2013, pp. 99-110.
44. S. Goren, O. Ozkurt, A. Yildiz, H. Fatih Ugurdag, **R. S. Chakraborty** and D. Mukhopadhyay, "Partial Bitstream Protection for Low-cost FPGAs with PUFs, Obfuscation & DPSR-LD", *Computers and Electrical Engineering* (*Elsevier*), vol. 39, no. 2, Feb. 2013, pp. 386-397.
45. R. Naskar and **R. S. Chakraborty**, "Performance of Reversible Digital Image Watermarking under Error-prone Data Communication: a Simulation-based Study", *IET Image Processing*, vol. 6, no. 6, Aug. 2012, pp. 728-737.
46. R. Naskar and **R. S. Chakraborty**, "Reversible Watermarking Utilizing Weighted–median based Prediction", *IET Image Processing*, vol. 6, no. 5, Jul. 2012, pp. 507-520.

47. S. Narasimhan, S. Bhunia and **R. S. Chakraborty**, "Hardware IP Protection During Evaluation Using Embedded Sequential Trojan", *IEEE Design & Test of Computers*, vol. 29, no. 3, Jun. 2012, pp. 70-79.
48. **R. S. Chakraborty** and S. Bhunia, "Security Against Hardware Trojan Attacks Using Key-based Design Obfuscation", *Journal of Electronic Testing*: *Theory and Applications* (*Springer*), vol. 27, no. 6, pp. 767-785, Dec. 2011.
49. **R. S. Chakraborty**, S. Paul, Y. Zhou and S. Bhunia, "Low-Power Hybrid CMOS-NEMS FPGA: Circuit Level Analysis and Defect-Aware Mapping", *IET Computers & Digital Techniques*, vol. 3, no. 6, pp. 609-624, Nov. 2009.
50. **R. S. Chakraborty** and S. Bhunia, "*HARPOON*: A SoC Design Methodology for Hardware Protection through Netlist Level Obfuscation", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 10, pp. 1493-1502, Oct. 2009.
51. **R. S. Chakraborty** and S. Bhunia, "A Study of Asynchronous Design Methodology for Robust CMOS-Nano Hybrid System Design", *ACM Journal of Emerging Technologies in Computing Systems*, vol. 5, no. 3, pp. 1-22, Aug. 2009.
52. **R. S. Chakraborty,** S. Narasimhan and S. Bhunia, "Hybridization of CMOS with CNT-Based Nano Electromechanical Switch for Low Leakage and Robust Circuit Design Using Nanoscaled CMOS Devices", *IEEE Transactions on Circuits and Systems I*, vol. 54, no. 11, pp. 2480-2488, Nov. 2007.

- **Conference Papers/Posters** (in reverse chronological order)
  1. **[Best Paper Award]** D. Das, R. Naskar and **R. S. Chakraborty**, "Linear and Non-Linear Filter-based Counter-Forensics Against Image Splicing Detection", *International Conference on Computer Vision & Image Processing* (*CVIP*), Nagpur, India, 2022.
  2. A. Saha, U. Chatterjee, D. Mukhopadhyay and **R. S. Chakraborty**, "DIP Learning on CAS-Lock: Using Distinguishing Input Patterns for Attacking Logic Locking", *Design, Automation and Test in Europe* (*DATE*) 2022, Antwerp, Belgium.
  3. A. Saha, D. Mukhopadhyay and R. S. Chakraborty, "(Extended Abstract) Design and Analysis of Logic Locking Techniques", *IFIP/IEEE International Conference on Very Large Scale Integration* (*VLSI-SoC*), Singapore, 2021.
  4. **[Best Paper Nomination]** P. Santikellur, R. Mukherjee and **R. S. Chakraborty**, "APUF-BNN: An Automated Framework for Efficient Combinational Logic Based Implementation of Arbiter PUF through Binarized Neural Network", *ACM Great Lakes Symposium on VLSI* (*GLSVLSI*), Virtual Conference, 2021.
  5. D. B. Tariang, S. C. Birudaraju, R. Naskar, V. Khare and **R. S. Chakraborty**, "Malware Classification Through Attention Residual Network based Visualization", *IEEE Asian Hardware Oriented Security and Trust* (*AsianHOST*), Kolkata, India, 2020.
  6. P. Ghosh, U. J. Botero, F. Ganji, D. Woodard, **R. S. Chakraborty** and D. Forte, "Automated Detection and Localization of Counterfeit Chip Defects by Texture Analysis in Infrared (IR) Domain", *IEEE International Conference on Physical Assurance and Inspection of Electronics* (*PAINE*), Washington, D.C., USA, 2020.
  7. U. Chatterjee, R. Sadhukhan, D. Mukhopadhyay, **R. S. Chakraborty**, D. Mahata and M. Prabhu, "*Stupify*: A Hardware Countermeasure of KRACKs in WPA2 using Physically Unclonable Functions", *The Web Conference* (*WWW*), Taipei, Taiwan, 2020.

8. V. S. Balijabudda, D. Thapar, P. Santikellur, **R. S. Chakraborty** and I. Chakrabarti, "Design of a Chaotic Oscillator based Model Building Attack Resistant Arbiter PUF", *IEEE Asian Hardware Oriented Security and Trust Symposium* (*AsianHOST*), Xi'an, P.R. China, 2019.
9. P. Santikellur, Lakshya, S. R. Prakash and **R. S. Chakraborty**, "A Computationally Efficient Tensor Regression Network based Modeling Attack on XOR Arbiter PUF", *IEEE Asian Hardware Oriented Security and Trust Symposium* (*AsianHOST*), Xi'an, P.R. China, 2019.
10. S. Chattopadhyay and **R. S. Chakraborty**, "Cyclic Beneš Network based Logic Encryption for Mitigating SAT-Based Attacks", *IEEE International Conference on Computer Design* (*ICCD*), Abu Dhabi, U.A.E., 2019.
11. S. Chattopadhyay, P. Kumari, B. Ray and **R. S. Chakraborty**, "Machine Learning Assisted Accurate Estimation of Usage Duration and Manufacturer for Recycled and Counterfeit Flash Memory Detection", *IEEE Asian Test Symposium* (*ATS*), Kolkata, India, 2019.
12. K. Bagadia, U. Chatterjee, D. B. Roy, D. Mukhopadhyay and **R. S. Chakraborty**, "Revisiting the Security of LPN based RFID Authentication Protocol and Potential Exploits in Hardware Implementations", *International Conference on Security, Privacy and Applied Cryptographic Engineering* (*SPACE*), Gandhinagar, India, 2019.
13. V. Govindan, S. Koteshwara, A. Das, Keshab K. Parhi and **R. S. Chakraborty**, "ProTro: A Probabilistic Counter based Hardware Trojan Attack on FPGA based MACSec enabled Ethernet Switch", *International Conference on Security, Privacy and Applied Cryptographic Engineering* (*SPACE*), Gandhinagar, India, 2019.
14. P. Ghosh, F. Ganji, D. Forte, D. L. Woodard and **R. S. Chakraborty**, "Automated Framework for Unsupervised Counterfeit Integrated Circuit Detection by Physical Inspection", *IEEE International Conference on Physical Assurance and Inspection of Electronics* (*PAINE*), Washington, D.C., USA, 2019.
15. D. B. Tariang, **R. S. Chakraborty**, R. Naskar, A. Roy and P. Sengupta, "Improved Detection and Localization for Copy-move Forgery Detection with Similar but Genuine Objects", *IEEE Conference on Computer Vision and Pattern Recognition Workshops* (*CVPRW*), Long Beach, California, USA, 2019.
16. U. Chatterjee, P. Santikellur, R. Sadhukhan, V. Govindan, D. Mukhopadhyay and **R. S. Chakraborty**, "United We Stand: A Threshold Signature Scheme for Identifying Outliers in PLCs (poster with 2 page short-paper)", Late Breaking Results (LBR) track of *IEEE/ACM Design Automation Conference* (*DAC*), Las Vegas, Nevada, USA, 2019.
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37. A. Palchaudhuri and **R. S. Chakraborty**, "Automated Design of High Performance Integer Arithmetic Cores on FPGA", EUROMICRO Digital System Design Conference (*DSD*), Funchal, Portugal, 2015.
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39. P. H. Nguyen, D. P. Sahoo, **R. S. Chakraborty** and D. Mukhopadhyay, "Cryptanalysis of Robust Ring Oscillator PUF with Enhanced Challenge-Response Set", *Design, Automation and Test in Europe* (*DATE*) 2015, Grenoble, France.
40. A. Palchaudhuri and **R. S. Chakraborty**, "Architecture and Design Automation of High Performance Arithmetic Architectures on FPGAs (poster)", *International Conference on VLSI Design* (*VLSID*) 2015, Bangalore, India.
41. **[Best Poster Award]** A. Palchaudhuri and **R. S. Chakraborty**, "High Performance Integer Arithmetic Circuit Design on Reconfigurable Computing Platforms (poster)", *International Conference on High Performance Computing* (*HiPC*) 2014, Goa, India.
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44. A. Palchaudhuri, **R. S. Chakraborty**, Md. Salman, S. Kardas and D. Mukhopadhyay, "Highly Compact Automated Implementation of Linear CA on FPGAs", *Cellular Automata for Research and Industry* (*ACRI*) 2014, Krakow, Poland. Published in *Lecture Notes on Computer Science*, vol. 8751, pp. 388-394, 2014.
45. D. P. Sahoo. S. Saha, D. Mukhopadhyay, **R. S. Chakraborty** and H. Kapoor, "Composite PUF: A New Design Paradigm for Physically Unclonable Functions on FPGA", *IEEE International Symposium on Hardware-Oriented Security and Trust* (*HOST*) 2014, Washington, D.C., USA.
46. R. Naskar and **R. S. Chakraborty**, "On Complexities of Spatial-Domain Reversible Watermarking Algorithms", *International Conference on Computing (INDIACom)* 2014, New Delhi, India.
47. R. Naskar, A. Raju, **R. S. Chakraborty**, "A Single Pass, High Throughput Reversible Watermarking Scheme for Audio based on Redundant Embedding", *International Conference on Signal Processing and Communication* (*ICSPC*) 2013, Noida, India.
48. D. P. Sahoo, D. Mukhopadhyay and **R. S. Chakraborty**, "Design of Low Area-overhead Ring Oscillator PUF with Large Challenge Space", *International Conference on Reconfigurable Computing and FPGAs* (*ReConFig*) 2013, Cancun, Mexico.
49. D. P. Sahoo, D. Mukhopadhyay and **R. S. Chakraborty**, "Formal Design of Composite Physically Unclonable Function", *Security Proofs for Embedded Systems* (*PROOFS*) 2013, Santa Barbara, California, USA (co-located with *CHES*'13).

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53. R. Naskar and **R. S. Chakraborty**, "Lossless Secret Image Sharing based on Generalized–LSB Replacement", *ACM Research in Applied Computation Symposium* (*RACS*) 2012, San Antonio, Texas, USA.
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58. **R. S. Chakraborty,** S. Narasimhan and S. Bhunia, "Embedded Software Security through Key-based Control Flow Obfuscation", *International Conference on Security Aspects in Information Technology, High-performance Computing and Networking* (*InfoSecHiComNet*) 2011, Haldia, West Bengal, India. Published in *Lecture Notes in Computer Science*, vol. 7011, pp. 30-44, 2011.
59. S. Bandyopadhyay, R. Naskar and **R. S. Chakraborty**, "Reversible Watermarking Using *Priority Embedding* through Repeated Application of *Integer Wavelet Transform*", *International Conference on Security Aspects in Information Technology, High-performance Computing and Networking* (*InfoSecHiComNet*) 2011, Haldia, West Bengal, India. Published in *Lecture Notes in Computer Science*, vol. 7011, pp. 45-56, 2011.
60. S. Narasimhan, X. Wang, D. Du, **R. S. Chakraborty** and S. Bhunia, "TeSR: A Robust Temporal Self-Referencing Approach for Hardware Trojan Detection", *IEEE International Symposium on Hardware-Oriented Security and Trust* (*HOST*) 2011, San Diego, CA, USA.
61. S. Bandyopadhyay, R. Naskar and **R. S. Chakraborty**, "Reversible Digital Watermarking using Integer Wavelet Transform", *International Conference on Scientific Paradigm Shift in Information Technology and Management* 2011, Kolkata, India.

62. S. Ali, D. Mukhopadhyay, **R. S. Chakraborty** and S. Bhunia, "Multi-level Attack: an Emerging Threat Model for Cryptographic Hardware", *Design, Automation and Test in Europe* (*DATE*) 2011, Grenoble, France.
63. D. Du, S. Narasimhan, **R. S. Chakraborty** and S. Bhunia, "Self-referencing: a Scalable Side-channel Approach for Hardware Trojan Detection", *Workshop on Cryptographic Hardware and Embedded Systems* (*CHES*) 2010, Santa Barbara, CA, USA. Published in *Lecture Notes in Computer Science*, vol. 6225, pp. 173-187, 2010.
64. **R. S. Chakraborty,** S. Narasimhan and S. Bhunia, "Embedded Software Security through Key-based Obfuscation (poster)", *Workshop on Cryptographic Hardware and Embedded Systems* (*CHES*) 2010, Santa Barbara, CA, USA.
65. **[Best Paper Nomination]** S. Narasimhan, D. Du, **R. S. Chakraborty**, S. Paul, F. Wolff, C. Papachristou, K. Roy and S. Bhunia, "Multiple-parameter Side-channel Analysis: a Non-invasive Hardware Trojan Detection Approach", *IEEE International Symposium on Hardware-Oriented Security and Trust* (*HOST*) 2010, Anaheim, CA, USA.
66. S. Narasimhan, S. Paul, **R. S. Chakraborty**, F. Wolff, C. Papachristou, D. J. Weyer and S. Bhunia, "System Level Self-Healing for Parametric Yield and Reliability Improvement under Power Bound", *NASA/ESA Conference on Adaptive Hardware and Systems* (*AHS*) 2010, Anaheim, CA, USA.
67. **R. S. Chakraborty** and S. Bhunia, "RTL Hardware IP Protection Using Key-Based Control and Data Flow Obfuscation", *International Conference on VLSI Design* (*VLSID*) 2010, Bangalore, India.
68. **R**. **S. Chakraborty**, S. Narasimhan and S. Bhunia, "Hardware Trojan: Threats and Emerging Solutions (invited paper)", *IEEE International High Level Design Validation and Test Workshop* (*HLDVT*) 2009, San Francisco, CA, USA.
69. **R. S. Chakraborty** and S. Bhunia, "Security Against Hardware Trojan Through a Novel Application of Design Obfuscation", *IEEE/ACM International Conference on Computer-aided Design* (*ICCAD*) 2009, San Jose, CA, USA.
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72. **R. S. Chakraborty** and S. Bhunia, "Hardware Protection and Authentication Through Netlist-level Obfuscation", *IEEE/ACM International Conference on Computer-aided Design* (*ICCAD*) 2008, San Jose, CA, USA.
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76. **R. S. Chakraborty**, S. Paul, and S. Bhunia, "Analysis and Robust Design of Diode-Resistor Based Nanoscale Crossbar PLA Circuits", *International Conference on VLSI Design* (*VLSID*) 2008, Hyderabad, India.
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78. **R. S. Chakraborty** and S. Bhunia, "Micropipeline-Based Asynchronous Design Methodology for Robust System Design Using Nanoscale Crossbar", *International Symposium on Quality Electronic Design* (*ISQED*) 2008, San Jose, CA, USA.
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- **Tutorials and Invited Talks** (in reverse chronological order)
  1. **R.S. Chakraborty**, J. Mathew and P. Santikellur, "Physically Unclonable Functions: Design, Applications and Threats", *IEEE International Technical Conference of IEEE Region 10* (*IEEE TENCON*), Oct. 2019, Kochi, India.
  2. D. J. Forte and **R. S. Chakraborty**, "Counterfeit Integrated Circuits: Threats, Detection, and Avoidance", *Cryptographic Hardware and Embedded Systems* (*CHES*), Sep. 2018, Amsterdam, The Netherlands.
  3. **R. S. Chakraborty**, "Hardware Trojans and Physically Unclonable Functions", *Hardware Security and Its Applications* (*HSA*), Mar. 2018, NIT Durgapur, India.
  4. **R. S. Chakraborty**, "Physically Unclonable Function: an Important Hardware Security Primitive", *Instruction Enhanced Program on IoT for Structural Health Monitoring*, Mar. 2018, IIT Kharagpur, India.
  5. **R. S. Chakraborty**, "Counterfeit ICs: Prevention and Detection through Circuit Design and Image Processing", *IEEE International Symposium on Devices, Circuits and Systems* (*ISDCS*), Mar. 2018, IIEST Shibpur, India.
  6. **R. S. Chakraborty** and P. Mishra, "Hardware Intellectual Property (IP) Security and Trust: Challenges and Solutions", *International Conference on VLSI Design* (*VLSID*), Jan. 2018, Pune, India.
  7. **R. S. Chakraborty**, "Physically Unclonable Function: an Important Hardware Security Primitive", *Workshop on Applied Security*, Nov. 2017, Scientific Analysis Group (SAG), DRDO, Delhi, India.
  8. **R. S. Chakraborty**, "Hardware Trojans: a Great Threat to National Security", *Workshop on Applied Security*, Nov. 2017, Scientific Analysis Group (SAG), DRDO, Delhi, India.
  9. **R. S. Chakraborty**, "Research on Digital Image Forensics at SEAL, IIT Kharagpur", *Cyber Security Awareness Week* (CSAW), Nov. 2017, IIT Kanpur, India.

10. **R. S. Chakraborty**, "Security in Embedded Systems", *3rd SERB School on Robotics*, Jun. 2017, IIT Delhi, India.
11. **R. S. Chakraborty**, "Physically Unclonable Functions", *GIAN Course on* "*Internet-of-Things Security: Issues, Innovations and Interplays*", Dec. 2016, IIT Patna, India.
12. **R. S. Chakraborty**, "Strict Avalanche Criterion and its Implications on PUF Security", *1st IEEE International Verification and Security Workshop* (IVSW), Jul. 2016, Sant Feliu de Guixols, Catalunya, Spain.
13. **R. S. Chakraborty**, "Combined Cryptanalysis and Machine Learning based Modeling Attack on LSPUFs", Special Session on "New Directions in Hardware Security", *IEEE International Conference on VLSI Design* (*VLSID*), Jan. 2016, Kolkata, India.
14. **R. S. Chakraborty**, D. Mukhopadhyay, P. H. Nguyen and D. P. Sahoo, "Physically Unclonable Function: a Promising Security Primitive for Internet-of-Things", *IEEE International Conference on VLSI Design* (*VLSID*), Jan. 2015, Bangalore, India.
15. **R. S. Chakraborty**, "Physically Unclonable Function: an Important Hardware Security Primitive", *3rd National Knowledge Network* Workshop, Dec. 2014, Guwahati, India.
16. **R. S. Chakraborty** and P. H. Nguyen, "Lightweight Physically Unclonable Functions: Design and Security Analysis", *International Conference on Security, Privacy and Applied Cryptography Engineering* (*SPACE*), Oct. 2014, Pune, India.
17. **R. S. Chakraborty**, "Hardware Trojans and Physically Unclonable Functions", *International Conference on Advances in Computing and Communication* (*ACC*), Kochi, August 2014.
18. **R. S. Chakraborty** and R. Naskar, "Reversible Watermarking", *International Conference on Information Systems Security* (*ICISS*), Dec. 2012, Guwahati, India.
19. **R. S. Chakraborty**, "Hardware Trojans: Threats and Emerging Solutions", *International Conference on Information Systems Security* (*ICISS*), Dec. 2011, Kolkata, India.
20. D. Mukhopadhyay and **R. S. Chakraborty**, "Testability of *Cryptographic Hardware* and Detection of *Hardware Trojans*", *IEEE Asian Test Symposium* (*ATS*), Nov. 2011, New Delhi, India.
21. D. Mukhopadhyay and **R. S. Chakraborty,** "Information Security from a Hardware Perspective: Challenges and Solutions", *IEEE International Workshop on Information Security* (*WIFS*), Nov. 2011, Foz do Iguacu, Brazil.
22. D. Mukhopadhyay, **R. S. Chakraborty** and C. Rebeiro, "Hardware Security: a 21st Century Perspective", *International Conference on VLSI Design* (*VLSID*), Jan. 2011, Chennai, India.

- **Patents/Invention Disclosures**
  1. A. Johnson, **R. S. Chakraborty**, D. Mukhopadhyay and C. Irani, "System and Method for Dynamic Partial Reconfiguration of Circuits Mapped or Configured on FPGA Platform", Indian Patent # 417967, Jan. 2023 (granted).
  2. R. S. Chakraborty, R. Naskar, **B. Sarkar**, "A Method and System for Evaluation of Reversible Watermarking of Digital Images and Audio", Indian Patent #405072, Aug. 2022 (granted).
  3. D. P. Sahoo, D. Mukhopadhyay, P. H. Nguyen and **R. S. Chakraborty**, "A Multiplexer based System for Electronic Device Authentication and Preventing Counterfeiting of the Electronic Device", Indian patent filed in July 2017 (Ref.: Application No. TEMP/E-1/27062/2017-KOL).

4. J. Mathew, **R. S. Chakraborty**, Y. Yang, A. M. Jabir and D. K. Pradhan, "Circuits and Methods for Memristor based Physically Unclonable Function", U.S. patent filed in November 2015 (Ref.: Application No. **14948617**).
5. **R. S. Chakraborty** and A. Palchaudhuri, "Architecture and Design Automation of High Performance Large Adders and Counters on FPGA through Constrained Placement", International PCT application filed in April 2014 (Ref: PCT/IB2014/060372). Indian Patent filed in February 2014 (Ref: 179/KOL/2014).
6. **R. S. Chakraborty** and B. K. Diddi, "Multi-level Inline Data Deduplication", U.S. patent #9,311,323, April 2016 (granted). International PCT application filed in October 2012 (Ref: PCT/IB2012/055688). Indian patent filed in September 2012 (Ref: 1022/KOL/2012).
7. **R. S. Chakraborty**, S. Narasimhan and S. Bhunia, "Protection of Intellectual Property Cores Through a Design Flow", U.S. patent #8402401, March 2013 (granted).
8. **R. S. Chakraborty**, F. Wolff, S. Paul, C. Papachristou and S. Bhunia: "A Statistical Approach to Hardware Trojan Detection using N-Detect Tests and Coverage Estimation using Random Sampling", Invention Disclosure, Case Western Reserve University, April 2009.

RESEARCH FUNDING

- **Central Power Research Institute (CPRI), Govt. of India**
  Project Title: "Cyber Security of Power Systems through Design-for Prevention, Real-time Detection and Effective Intervention"
  PI: Prof. Dipanwita Roy Chowdhury
  Co-PI: Prof. Pabitra Mitra, Prof. Ashok Pradhan, Dr. Rajat Subhra Chakraborty
  Duration: 1 years (Mar 2022 – Mar 2023)

- **Science and Engineering Research Board (SERB), Govt. of India**
  Project Title: "A Comprehensive Framework for Adversarial Evaluation of Random Number Generators: Theory and Implementation"
  PI: Dr. Rajat Subhra Chakraborty
  Duration: 3 years (Jan 2020 – Jan 2023)

- **Intel Corporation**
  Project Title: "DeepFake Catcher: Methods to Identify AI Generated Facial Videos and Images"
  PI: Dr. Rajat Subhra Chakraborty
  Duration: 15 months (Oct 2019 – Jan 2021)

- **Indira Gandhi Centre For Atomic Research (IGCAR), Government of India, Department of Atomic Energy, Govt. of India**
  Project Title: "Design and Development of FPGA Implementable Physical Unclonable Function for High Security Authentication Applications"
  PI: Dr. Rajat Subhra Chakraborty
  Co-PI: Prof. Indrajit Chakrabarti
  Duration: 3 years (May 2019 – May 2022)

- **Department of Science and Technology, Govt. of India**

Project Title: "Digital Image Forensics in the Context of a Connected India: Algorithms and Implementation"
PI: Dr. Rajat Subhra Chakraborty
Co-PI: Dr. Ruchira Naskar (IIEST Shibpur)
Duration: 3 years (Jul 2019 - Mar 2023)

- **Directorate of Futuristic Technology Management (DFTM), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
  Project Title: "Secure Resource-Constrained Communication Framework for Tactical Networks Using Physically Unclonable Functions (SeRFPUF)"
  PI: Dr. Debdeep Mukhopadhyay
  Co-PI: Dr. Rajat Subhra Chakraborty
  Duration: 5 years (Jul 2017 - Jul 2022)

- **Hindustan Aeronautics Limited, Ministry of Defence, Govt. of India**
  Project Title: "Design, Implementation & Evaluation of Encryption/Decryption Unit for IFF System"
  PI: Dr. Debdeep Mukhopadhyay
  Co-PI: Dr. Rajat Subhra Chakraborty
  Duration: 2 years (Jan 2017 - Jan 2019)

- **Intel Corporation (U.S.A.)**
  Project Title: "Verification Challenges in Compression and Cryptographic Stacks in *QuickAssist* Technology"
  PI: Dr. Rajat Subhra Chakraborty
  Duration: 4 years (May 2016 - May 2020)

- **BRNS, Dept. of Atomic Energy, Govt. of India**
  Project Title: "Hardware Security in the Context of a Connected World: Threats and Mitigations"
  PI: Dr. Rajat Subhra Chakraborty
  Co-PI: Dr. Debdeep Mukhopadhyay
  Duration: 3 years (May 2016 - May 2019)

- **IBM**
  Project Title: "Optimize real time encryption performance for high volume storage data traffic by means of software improvements to Linux"
  PI: Dr. Rajat Subhra Chakraborty
  Duration: 3 years (November 2015 - November 2018)

- **DEITY, Ministry of Communication and IT, Govt. of India**
  Project Title: "Information Security Education and Awareness (ISEA) Project Phase-II"
  PI: Dr. Debdeep Mukhopadhyay
  Co-PI: Dr. Sandip Chakraborty and Dr. Rajat Subhra Chakraborty
  Duration: 5 years (November 2015 - November 2020)

- **Wipro Limited, India**
  Project Title: "Securing Internet-of-Things using Unconventional Cryptographic Techniques"
  PI: Dr. Debdeep Mukhopadhyay and Dr. Rajat Subhra Chakraborty

Duration: 4 years (June 2015 - June 2019)

- **Science and Engineering Research Board (SERB), Govt. of India**
  Project Title: "High Performance Reversible Watermarking of Digital Images: Theory, Implementation and Impact on Medical Imaging"
  PI: Dr. Rajat Subhra Chakraborty
  Duration: 3 years (May 2014 - May 2017)

- **Scientific Analysis Group (SAG), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
  Project Title: "Power Attacks on Stream Ciphers and Cache Memory Attacks"
  PI: Dr. Debdeep Mukhopadhyay
  Co-PI: Dr. Rajat Subhra Chakraborty
  Duration: 2 years (Mar. 2013 - Mar. 2015)

- **Reconnoiter Technology and Research, India**
  Project Title: "Hardware Trojan Attack Testbed on FPGA based Systems" (consultancy project)
  PI: Dr. Rajat Subhra Chakraborty
  Co-PI: Dr. Debdeep Mukhopadhyay
  Duration: 3 years (Dec. 2012 - Dec. 2015)

- **Centre for Artificial Intelligence and Robotics (CAIR), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
  Project Title: "Machine Learning based Model-building Attack on PUFs"
  PI: Dr. Rajat Subhra Chakraborty
  Co-PI: Dr. Debdeep Mukhopadhyay
  Duration: 2 years (Dec. 2012-Dec.2014)

- **Centre for Artificial Intelligence and Robotics (CAIR), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
  Project Title: "Study of Hardware Malware Vulnerabilities and Mitigation Techniques for FPGAs" (completed)
  PI: Dr. Rajat Subhra Chakraborty
  Co-PI: Dr. Debdeep Mukhopadhyay
  Duration: 2 years (Sep. 2010-Aug.2012)

- **Centre for Artificial Intelligence and Robotics (CAIR), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
  Project Title: "Design of Controller for Finite Field Arithmetic on FPGAs" (as co-PI)
  PI: Dr. Debdeep Mukhopadhyay
  Co-PI: Dr. Rajat Subhra Chakraborty
  Duration: 2 years (Oct. 2010-Sep.2012)

- **Sponsored Research and Industrial Consultancy (SRIC), IIT Kharagpur**
  Project Title: "Hardware Security: Ensuring TRUST in Integrated Circuits"
  PI: Dr. Rajat Subhra Chakraborty
  Duration: 2 years (Sep. 2010-Aug.2012)

CURRENT GRADUATE STUDENTS

- **Ph.D.:** B. V. Sreekanth (joint supervisor), Rijoy Mukherjee, Akashdeep Saha (joint supervisor), Kuheli Pratihar (joint supervisor), M. Sivappriya (joint supervisor)
- **M.S.:** Pallavi Anand, Sumitava Biswas (joint supervisor), Sneha Swaroopa

PAST GRADUATE STUDENTS

- **Ph.D.:**
  - Pranesh Santikellur (2022) – (currently Senior Embedded Security Researcher at Technology Innovation Institute, Abu Dhabi, U.A.E.)
    Thesis: "Design and Analysis of Machine Learning based Modeling Attacks on Strong Physically Unclonable Functions"
  - Diangarti Bhalang Tariang (2022) – (currently Post-doctoral Researcher, University Frederico II of Naples, Italy)
    Thesis: "Deep Learning-based Multimedia Forensics and Malware Classification"
  - Urbi Chatterjee (2020, co-supervisor: Debdeep Mukhopadhyay) – (currently Assistant Professor, IIT Kanpur, India).
    Thesis: "Design, Analysis and Implementation of Physically Unclonable Function based Authentication Frameworks for Internet-of-Things"
  - Durga Prasad Sahoo (2017, co-supervisor: Debdeep Mukhopadhyay) – (currently Cyber Security Specialist at Robert Bosch Limited, Bangalore, India)
    Thesis: "Design and Analysis of Secure Physically Unclonable Function Compositions"
  - Anju Johnson (2016, co-supervisor: Debdeep Mukhopadhyay) – (currently Senior Lecturer at University of Huddersfield, U.K.).
    Thesis: "Remote Dynamic Partial Reconfiguration for Emerging IoT Applications: Threats and Countermeasures"
  - Ruchira Naskar (2014) – (currently Assistant Professor, IIEST Shibpur, Howrah, India).
    Thesis: "Reversible Watermarking for Digital Images: Algorithms and Implementations"

- **M.S. (through Research):**
  - Vidya Govindan (2019) (currently Senior Engineer at Qualcomm, Bangalore, India)
    Thesis: "FPGA based Hardware Trojan: Design, Implementation and Detection"
  - Pallabi Ghosh (2019) (currently Ph.D. student at University of Florida at Gainesville, U.S.A.)
    Thesis: "Counterfeit Integrated Circuit Detection using Image Processing Techniques"
  - Aniket Roy (2018) (currently Ph.D. student at Johns Hopkins University, U.S.A.).
    Thesis: "Multimedia Security Through Reversible Image Watermarking and Digital Image Forensics"
  - Sayandeep Saha (2016, co-supervisor: Debdeep Mukhopadhyay).
    Thesis: "Improved ATPG Techniques and Testability Based Metrics for Hardware Trojan Horses"
  - Ayan Palchaudhuri (2014) – (currently Assistant Professor, IIT Bhubaneswar).
    Thesis: "Architecture and Design Automation of High Performance Integer Arithmetic Soft Cores on Xilinx Field Programmable Gate Arrays"
  - Indrasish Saha (2013) – (currently Senior Lead Engineer at Qualcomm, Bangalore, India).
    Thesis: "Attacks on FPGA-based System Implementations".

TEACHING

- **Courses Taught:** Programming and Data Structures (CS11001), Programming and Data Structures Laboratory (CS19001), Switching Circuits and Logic Design (CS21002), Switching Laboratory (CS29002), Computer Networks (CS31006), Networks Lab (CS39006/CS49001), Computer Organization and Architecture (CS31007), Computer Organization Laboratory (CS39001), Computer Architecture and Operating System (CS31702), Cryptography and Network Security (CS60065), VLSI System Design (CS60067, IC 80103), Hardware Security (CS60004), Computing Systems Laboratory (IC89002), M.Tech. Seminar-I (IC89003).

Note: course numbers starting with "6" or higher are PG courses, rest are UG courses.

PROFESSIONAL INVOLVEMENTS

- **Associate Editor:** *IEEE Transactions on CAD* (2018 onward), *IEEE Transactions on Multi-scale Computing Systems* (till 2018), *Journal of Electronic Testing and Test Applications* (Springer JETTA, 2020-)
- **General Co-chair:** *IEEE AsianHOST'20*
- **Program Co-Chair**: *SPACE*'15, *SPACE*'14, *DSD-AHSA*'17, *DSD-AHSA'*20
- **Tutorial Co-chair**: *VLSID'*18, *ATS*'19
- **Assistant Secretary**: IEEE Kharagpur Section, (Jan. 2021 – present)
- **Guest Editor**: Special issue on "Secure and Fault Tolerant Embedded Computing" in *ACM Transactions on Embedded Computing Systems* (Sep. 2017)
- **Journal Reviewer:** *Proceedings of the IEEE; IEEE Transactions on Information Forensics and Security; IEEE Transactions on Industrial Informatics; IEEE Transactions on CAD; IEEE Transactions on Dependable and Secure Computing; IEEE Design & Test*; *IEEE Transactions on Circuits and Systems*-I; *IEEE Transactions on Circuits and Systems*-II; *IEEE Transactions on VLSI; IEEE Transactions on Emerging Topics in Computing; IEEE Embedded Systems Letters; ACM Transactions on Design Automation of Electronic Systems; ACM Transactions on Embedded Computing Systems; ACM Journal of Emerging Technologies in Computing Systems*; *ACM Transactions on Multimedia Computing, Communications and Applications; IET Circuits, Devices and Systems*; *IET Computers and Digital Techniques*; *Integration, The VLSI Journal* (*Elsevier*); *Digital Signal Processing* (*Elsevier*); *Journal of Electronic Testing: Theory and Applications* (*Springer*); *Journal of Hardware and Systems Security* (*Springer*)
- **Book Reviewer**: Book series titled *Synthesis Lectures on Information Security, Privacy, and Trust* (*Morgan Claypool*).
- **Academic Judge**: *IEEE E.J. McCluskey Best Doctoral Thesis Award Contest* (part of *VTS*'14), *DAC Ph.D. Forum* (2017, 2019).
- **Program Committee Member***: DAC* (2021), *CHES* (2021), *HOST* (2021), *VLSID* (2012-2019), *ICCD* (2015-2018), *GLSVLSI* (2019), *RFIDsec* (2015), *AsianHOST* (2016-2019), *AHSA* (part of *DSD*) (2014-2019), *VDAT* (2013-2014), *IEEE WRTLT* (2012-2017), *IEEE HOST* (2018), *ACM RACS* (2012), *VDAT* (2012-2019), *SPACE* (2011-2019), *ICISS* (2014-2017), *IEEE IVSW* (2016-2018), *ACM ASHES* (2017-2019).
- **Other Professional Involvement:** Invited by *IBM* to be part of the *IBM India Onward* initiative, *National Service Scheme* (NSS) Program Officer (January 2011 – December 2012).

PROFESSIONAL AND ACADEMIC HONORS

- Listed among the top 2% Computer Science researchers in the world (in the "Computer Hardware and Architecture" sub-field), in the "Single Calendar Year 2021" category, as described in the following publication: Ioannidis *et al.*, "September 2022 data-update for "Updated science-wide author databases of standardized citation indicators"", *Mendeley Data*, vol 4, Oct. 2022 (available here).
- Listed among the top 2% Computer Science researchers in the world (in the "Computer Hardware and Architecture" sub-field), in the "Single Calendar Year 2020" category, as described in the following publication: Baas *et al.*, "August 2021 data-update for "Updated science-wide author databases of standardized citation indicators"", *Mendeley Data*, vol. 3, Oct. 2021 (available here).
- Listed among the top 2% Computer Science researchers in the world (in the "Computer Hardware and Architecture" sub-field), in the "Single Calendar Year 2019" category, as described in the following publication: Ioannidis *et al.*, "Updated science-wide author databases of standardized citation indicators", *PLoS Biology*, 18(10), Oct. 2020 (available here).
- Recipient of Intel Unrestricted Research Grant Award, 2019.
- Recipient of *Outstanding Faculty Award* (*Associate Professor level*) from IIT Kharagpur, 2018.
- Recipient of *IEI Young Engineers Award*, 2016.
- Recipient of *Science and Engineering Research Board International Travel Support* grant to attend the *DSD Euromicro Conference* in Limassol, Cyprus, 2016.
- Recipient of *IBM Shared University Research* (SUR) *Award*, 2015.
- Recipient of *Royal Academy of Engineering* (U.K.) *Research Exchange Fellowship* award, 2014.
- Recipient of *Microsoft Research India* Unrestricted Research Grant of Rs. 100,000, 2013.
- Recipient of *Council of Scientific and Industrial Research International Travel Support* grant to attend the *RECONFIG* conference in Cancun, Mexico, 2013.
- Recipient of *IBM Faculty Award*, 2012.
- Recipient of *Department of Science and Technology International Travel Support* grant to attend the *IEEE WRTLT* workshop in Niigata, Japan, 2012.
- Invited to deliver a plenary session keynote talk on *Testing Techniques for Hardware Trojan Detection* in the *IEEE WRTLT* workshop in Niigata, Japan, 2012.
- Semi-finalist in the *IEEE E.J. McCluskey Best Doctoral Thesis Award Contest*, and invited to present (as part of the contest) at the *28th VLSI Test Symposium* (VTS) at Santa Cruz, CA, U.S.A., 2010.
- Recipient of *DAC Young Student Support Program* (YSSP) travel and attendance grant, awarded by ACM and IEEE, to attend the *46th Design Automation Conference* (DAC) at San Francisco, CA, U.S.A., 2009.
- Selected to present at the *ACM/SIGDA Ph.D Forum* at the *46th Design Automation Conference* (DAC) at San Francisco, CA, U.S.A., 2009.
- Recipient of the *Ruth Barber Moon Award for academic excellence and leadership promise* from the School of Graduate Studies, Case Western Reserve University, 2009.
- Recipient of the *Verhosek Fund Graduate Travel Assistance Award* from the Graduate Student Senate of Case Western Reserve University, 2009.

- Recipient of *Graduate Research Fellowship* (including full tuition waiver), Dept. of EECS, Case Western Reserve University, 2006-2007.
- Recipient of *Research Assistantship* (including full tuition waiver), Dept. of EECS, Case Western Reserve University, 2007-2010.
- Felicitated by the *Telegraph Education Foundation*, for securing the 10th Rank in the WBJEE (engineering entrance) examination, 2001, and 17th Rank in the Higher Secondary (12th Standard) Examination in the state, 2001 (out of approx. 40,000 candidates).
- Felicitated by Govt. of West Bengal, India, for securing the 17th Rank in the Higher Secondary (12th Standard) Examination in the state, 2001 (out of approx. 400,000 candidates).

PROFESSIONAL MEMBERSHIP

- Senior Member, IEEE
- Senior Member, ACM

OTHER INFORMATION

- Nationality: Indian
- Date of Birth: 3rd September 1982
- Gender: Male (He/Him/His)
- Married, with one daughter.