CURRICULUM VITAE

Name: **ANINDYA SUNDAR DHAR**

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Education: Ph. D. (Electronics and Electrical Communication Engineering),
Dissertation: Cordic based array architectures for electromedical signal processing
Indian Institute of Technology, Kharagpur, 1994.

M. Tech. (Electronics and Electrical Communucation Engineering),
Specialization: Integrated Circuits and Systems Engineering
Indian Institute of Technology, Kharagpur, 1989.

B. Tech. (Electronics and Telecommunication Engineering),
University of Calcutta (Bengal Engineering College), 1987.

Current Academic Position: March 2014 - till date: Professor,
Dept. of Electronics and Electrical Communication Engineering,
Indian Institute of Technology, Kharagpur

Previous Positions Held: 2007 - 2014: Associate Professor,
Dept. of Electronics and Electrical Communication Engineering,
Indian Institute of Technology, Kharagpur

1998 - 2007: Assistant Professor,
Dept. of Electronics and Electrical Communication Engineering,
Indian Institute of Technology, Kharagpur

1996 - 1998: Visiting Lecturer,
Dept. of Electronics and Electrical Communication Engineering,
Indian Institute of Technology, Kharagpur

1994 - 1996: Senior Project Officer,
Dept. of Electronics and Electrical Communication Engineering,
Indian Institute of Technology, Kharagpur

Academic/Administrative services (at Indian Institute of Technology, Kharagpur):

Present: Chairman of the Departmental Undergraduate Committee

Faculty in-charge of Integrated Circuits and Systems Engg. Lab.

Faculty-in-charge of Electronic Circuits Lab.

Faculty-in-charge of CAD Lab.

Past: 1998 - 2012 : Faculty advisor for Master's students in the specialization Microelectronics and VLSI Design

2000 - 2003 : Faculty-in-charge of Analog Design in the Advanced VLSI Design Lab. (also a founder member)

Sponsored Projects:

Present: Design of fault-tolerant VLSI systems for applications in satellite communication,
Sponsored by: Indian Space Research Organization
(as Principal Investigator)

Implementing a scalable video transcoder based on motion based on motion compensated temporal filtering, Sponsored by: Indian Space Research Organization
(as Co-Principal Investigator)

Past: Iron disilicide heterojunction solar cells,
Sponsored by: Dept. of Science and Technology, Govt. of India
(as Co-Principal Investigator)

Degradation and breakdown of metal gate / high-k / III-V semiconductor structures
Sponsored by: Dept. of Science and Technology, Govt. of India
(as Co-Principal Investigator)

Design and development of non-invasive blood glucose measuring system
Sponsored by: Dept. of Information Technology, Govt. of India
(as Co-Principal Investigator)

Investigations of CMOS device technologies for strain engineered MOSFETs using TCAD
Sponsored by: Dept. of Information Technology, Govt. of India
(as Co-Principal Investigator)

Technology CAD of nanomosfets in hybrid orientation
Sponsored by: Dept. of Science and Technology, Govt. of India
(as Co-Principal Investigator)

Design of high speed and/or low power adaptive decision feedback equalizers – an architectural optimization approach
Sponsored by: Dept. of Information Technology, Govt. of India
(as Co-Principal Investigator)

Non-invasive blood glucose measuring system
Sponsored by: Life Science Research Board, Govt. of India
(as Co-Principal Investigator)

Adaptive signal processing on block floating point arithmetic
Sponsored by: Dept. of Science and Technology, Govt. of India
(as Co-Principal Investigator)

Design of FPGA based realization of high speed adaptive equalizers
Sponsored By; Ministry of Human Resource and Development, Govt. of India
(as Co-Principal Investigator)

Development and analysis of algorithms for face detection, tracking and coding for videophones and video conferencing applications
Sponsored By; Ministry of Human Resource and Development, Govt. of India
(as Co-Principal Investigator)

Development of VLSI design laboratory
Sponsored by: IIT foundation, U.S.A.
(as Co-Principal Investigator)

Design and development of CORDIC based transmultiplexer and BPSK/QPSK modulator
Sponsored by: Indian Space Research Organization
(as Co-Principal Investigator)

Research Guidance (Ph.D. completed):

1. Suraiya Pervin (A class of pipelined architectures to realize high speed adaptive equalizers) [Jointly guided with Prof. M. Chakraborty] 2001.

2. Ashis Kumar Mal (Sampled analog architectures for real time signal processing) 2006.

3. Rajarshi Mahapatra (Link adaptive modulation techniques) [Joint guided with Prof. Debasish Datta] 2008.

4. Kailash Chandra Ray (CORDIC based VLSI architectures for real time digital signal processing) 2008.

5. B. Lakshmi (High speed VLSI CORDIC architectures) 2010.

6. Ayan Banerjee (VLSI architectures for Fourier transform based real time signal processing systems) [Jointly guided with Prof. S. R. Bhadra Chaudhuri] 2013.

7. Prajit Nandi (Performance enhancement of multi-axial resistive MEMS sensor by a novel signal processing scheme) [Joint guided with Prof. S. Das] 2014.

8. Amitava Ghosh (Low power techniques for integrated transceiver subsystem design for wireless sensor node communication) [Jointly guided with Dr. Achintya Halder] 2015.

Journal Publications:

1. A. S. Dhar and S. Banerjee, “An array architecture for fast computation of discrete Hartley transform”, *IEEE Trans. Circuits Systs.*, vol. 38, No. 9, pp. 1095 - 1098, Sep. 1991.

2. A. S. Dhar and S. Banerjee, “An array architecture for computing two-dimensional discrete Hartley transform”, *Computers Electrical Engng.*, vol. 17, No.1, pp. 23 - 29, 1991.

3. A. S. Dhar and S. Banerjee, “An array architecture for computing discrete Fourier transform to assist semiconductor device modelling”, *Electronics Letters*, vol. 28, No. 7, pp. 697 - 698, 26th March 1992.

4. S. Mittra, A. S. Dhar and S. Banerjee, “An array architecture for image reconstruction using the direct Fourier method”, *Computers Electrical Engng.*, vol. 20, No. 4, pp. 327 - 333, 1994.

5. M. C. Mandal, A. S. Dhar and S. Banerjee, “Multiplierless array architecture for computing discrete cosine transform”, *Computers Electrical Engng.*, vol. 21, No. 1, pp. 13 - 19, 1995.

6. A. Banerjee, A. S. Dhar and S. Banerjee, “FPGA realization of a CORDIC based FFT processor for biomedical signal processing”, *Microprocessors Microsysts.*, vol.25, No. 3, pp. 131 - 142, May 2001.

7. K. Maharatna, A. S. Dhar and S. Banerjee, “A VLSI array architecture for realization of DFT, DHT, DCT and DST”, *Signal Processing*, vol. 81, No. 9, pp. 1813 - 1822, Sep. 2001.

8. A. Banerjee and A. S. Dhar, “Novel architecture for QAM modulator–demodulator and its generalization to multicarrier modulation”, *Microprocessors Microsysts.*, vol.29, No. 7, pp. 351 - 357, Sep. 2005.

9. M. Chakraborty, A. S. Dhar and M. H. Lee, “A trigonometric formulation of the LMS algorithm for realization on pipelined CORDIC”, *IEEE Trans. Circuits Systs. II*, vol. 52, No. 9, pp. 530 - 534, Sep. 2005.

10. K. C. Ray and A. S. Dhar, “CORDIC-based unified VLSI architecture for implementing window functions for real time spectral analysis”, *IEE Proc. Circuits, Devices Syst.*, vol. 153, No. 6, pp. 539 - 544, Dec. 2006.

11. R. Mahapatra, A. S. Dhar and D. Datta, “On feasibility of a multiplier-less phase shifting scheme for digital phase modulation and its VLSI implementation”, *Int. J. Electron.*, vol. 94, No. 2, pp. 171 - 181, Feb. 2007.

12. K. C. Ray and A. S. Dhar, “High throughput VLSI architecture for Blackman windowing in real time spectral analysis”, *J. Comput.*, vol. 3, No. 5, pp. 54 - 59, May 2008.

13. R. Mahapatra, A. S. Dhar and D. Datta, “Adaptive digital phase modulation schemes using transition-initiated phase acceleration”, *Int. J. Electron. Commun.*, vol. 62, No. 10, pp. 740-753, Nov. 2008.

14. R. Mahapatra, A. S. Dhar and D. Datta, “Integrated voice and data transmission employing adaptive modulation in wireless networks”, *Int. J. Electron. Commun.*, vol. 63, No. 12, pp. 1012-1025, Dec. 2009.

15. K. Bhattacharyya, R. Biswas, A. S. Dhar and S. Banerjee, “Architectural design and FPGA implementation of radix-4 CORDIC processor”, *Microprocessors Microsysts.*, vol. 34, No. 2-4, pp. 96-101, Mar.-Jun. 2010.

16. B. Lakshmi and A. S. Dhar, “CORDIC architectures: A survey”, *VLSI Design*, ID 794891, 19 pages, 2010.

17. B. Lakshmi and A. S. Dhar, “VLSI architecture for low latency radix-4 CORDIC”, *Computers Electrical Engng*., vol. 37, No. 6, pp. 1032 - 1042, Nov. 2011.

18. S. M. Ghosh, A. S. Dhar and S. Bhunia, “Direct digital frequency synthesizer design with modified parabolic method”, *Int. J. Soft Comput. Engng*., vol. 1, No. 6, pp. 149 - 153, Jan. 2012.

19. A. Ghosh, A. Halder and A. S. Dhar, “A variable RF carrier modulation scheme for ultralow power wireless body-area network”, *IEEE Systs. J.*, vol. 6, No. 2, pp. 305 - 316, Jun. 2012.

20. A. S. Reddy and A. S. Dhar, “A discrete time continuous level VLSI architecture in current mode to implement discrete Haar wavelet transform”, *Analog Integrated Circuits Signal Process.*, vol. 73, No. 1, pp. 353 - 362, Oct. 2012.

21. A. Banerjee and A. S. Dhar, “Pipelined VLSI architecture using CORDIC for transform domain equalizer”, *J. Signal Process. Systs.*, vol. 70, No. 1, pp. 39 - 48, Jan. 2013.

22. B. Lakshmi and A. S. Dhar, “VLSI architecture for parallel radix-4 CORDIC”, *Microprocessors Microsysts.*, vol. 37, No. 1, pp. 79 - 86, Feb. 2013.

23. K. Ghosh and A. S. Dhar, “A fast VLSI architecture of a hierarchical block matching algorithm for motion estimation”, *J. Real-time Image Processing*, DOI 10.1007/s11554-012-0300-7, published online : 4 Jan. 2013.

24. K. C. Ray and A. S. Dhar, “CORDIC based VLSI architecture for implementing Kaiser-Bessel window in real time spectral analysis”, *J. Signal Process. Systs.*, vol. 74, No. 2, pp. 235 - 244, Feb. 2014.

25. P. Nandi, D. Sahu, A. S. Dhar, S. Das, “SPICE compatible behavioural modelling of resistive sensors”, *Meas. Sci. Technol.*, vol. 25, 055104, 13 pp., 2014.

26. P. Nandi, R. Biswas, A. S. Dhar, S. Das, “Novel architecture for measurements in resistive MEMS sensors”, *Meas. Sci. Technol.*, vol. 25, 055106, 17 pp., 2014.

27. A. Mukherjee and A. S. Dhar, “Real-time fault-tolerance with hot-standby topology for conditional sum adder”, *Microelectronics Realiability*, vol. 55, No. 3 - 4, pp. 704 - 712, Feb. - Mar. 2015.

28. R. Mukherjee, K. Seth, A. S. Dhar, I. Chakrabarti, S. Sengupta, “High performance VLSI architecture for three-step search algorithm”, *Circuits Syst. Signal Process.*, vol. 34, No. 5, pp. 1595 - 1612, May 2015.

29. M. Panigrahy, I. Chakrabarti and A. S. Dhar, “Low-delay parallel architecture for fractal image compression”, *Circuits Syst. Signal Process.*, DOI 10.1007/s00034-015-0088-3, published online: 4 Jun 2015.

Conference Publications:

1. A. S. Dhar and S. Banerjee, “Regular interconnection pattern between arrays for fast computation of discrete Hartley transform”, *Proc.* 3*rd Int. Workshop VLSI Design*, Bangalore, INDIA, pp. 283 -288, Jan. 1990.

2. A. S. Dhar and S. Banerjee, “An array architecture for computing KLT basis vectors”, *Proc.* 5*th Int. Conf. VLSI Design*, Bangalore, INDIA, pp. 167 - 170, 4-7 Jan. 1992.

3. A. S. Dhar and S. Banerjee, “Doppler ultrasonograph with CORDIC based spectrum analyzer for blood flow velocity estimation”, *Proc.* 14*th Conf. Biomed. Engg. Soc. India*, New Delhi, INDIA, pp. 2/107 - 2/108, 15-18 Feb. 1995.

4. K. Maharatna, A. S. Dhar and S. Banerjee, “A 52MHz 1.5V 16bit high performance shifter circuit”, *Proc.* 5*th Int. Conf. VLSI and CAD*, Seoul, KOREA, pp. 478 - 480, Oct. 1997.

5. P. Saranga Pani and A. S. Dhar, “Architecture for Haar wavelet transform based still image compression”, *Proc. Conf. Distributed Processing Networking*, Kharagpur, INDIA, pp. 54 - 58, Dec. 1997.

6. K. Maharatna, A. S. Dhar and S. Banerjee, “Design of macromodules using CORDIC for low power / low voltage DSP chips”, *Proc. Conf. Distributed Processing Networking*, Kharagpur, INDIA, pp. 129 - 132, Dec. 1997.

7. K. Maharatna, A. S. Dhar and S. Banerjee, “Low voltage / low power CORDIC based DHT chip implemented using transmission gate logic on sea-of-gates technology”, *Proc. Int. Conf. Computers Devices Commun.*, Calcutta, INDIA, pp. 154 - 157, Jan. 1998.

8. S. Pervin, M. Chakraborty and A. S. Dhar, “Pipelining the adaptive decision feedback equalizer with zero latency”, *Proc. Nat. Conf. Commun.*, New Delhi, INDIA, pp. 287 - 290, Jan. 2000.

9. M. Chakraborty, S. Pervin and A. S. Dhar, “Systolizing the adaptive decision feedback equalizer using a symbolic state space formulation”, *Proc. European Conf. Signal Processing*, Finland, pp. 263 - 266, Sept. 2000.

10. S. Pervin, A. S. Dhar and M. Chakraborty, “A pipelind architecture for KLT based LMS adaptive equalizer”, *Proc. Int. Conf. Commun., Computers and Devices*, Kharagpur, INDIA, pp. 615 - 618, Dec. 2000.

11. M. Chakraborty, A. S. Dhar and S. Pervin, “A trigonometric formulation of the LMS algorithm”, *Proc. Nat. Conf. Commun.*, Kanpur, INDIA, pp. 243 - 247, Jan. 2001.

12. M. Chakraborty, A. S. Dhar and S. Pervin, “CORDIC realization of the transversal adaptive filter using a trigonometric LMS algorithm”, *Proc. Int. Conf. Acoustics, Speech Signal Process.*, Utah, USA, pp. 1225 - 1228, 7-11 May 2001

13. S. Pervin, A. S. Dhar and M. Chakraborty, “A high speed CORDIC based architecture for the complex adaptive equalizer”, *Proc. Int. Conf. Energy, Automation Inf. Technol.*, Kharagpur, INDIA, pp. 182 - 185, Dec. 2001.

14. T. Sanjay and A. S. Dhar, “FPGA realization of a CORDIC based DHT processor for high throughput signal processing application”, *Proc. Int. Conf. Energy, Automation Inf. Technol.*, Kharagpur, INDIA, pp. 367 - 371, Dec. 2001.

15. A. K. Mal and A. S. Dhar, “Analog sampled data architecture for discrete Hartley transform”, *Proc. IEEE Region* 10 *Conf. Convergent Technol. Asia- Pacific* (*TENCON*), Bangalore, INDIA, pp. 1035 - 1039, 15-17 Oct. 2003.

16. A. K. Mal and A. S. Dhar, “Analog sampled data architecture for discrete cosine transform”, *Proc. Fifth Int. Conf. ASIC* (*ASICON*), Beijing, China, pp. 502 - 505, 21-24 Oct. 2003.

17. M. Sarma, D. Samanta and A. S. Dhar, “VLSI architecture for multi-resolution three step search algorithm”, *Proc. Fifth Int. Conf. ASIC* (*ASICON*), Beijing, China, pp. 918 - 921, 21-24 Oct. 2003.

18. A. K. Mal and A. S. Dhar, “Sampled analog architecture for discrete Hartley transform for prime N”, *Proc.* 10*th Int. Conf. Electronic Circuits Systs.* (*ICECS*), Sharjah, UAE, pp. 152 - 155, 14-17 Dec. 2003.

19. A. K. Mal and A. S. Dhar, “Switched capacitor architecture for prime length discrete Hartley transform” *Proc. Conf. Electron Dev. Solid State Circuits*, Hong Kong, pp. 505 - 508, 16-18 Dec. 2003.

20. A. K. Mal and A. S. Dhar, “Analog VLSI architecture for discrete cosine transform using dynamic switched capacitors”, *Proc.* 17*th Int. Conf. VLSI Design*, Mumbai, INDIA, pp. 666 - 669, 5-9 Jan. 2004.

21. A. Basu, A. K. Mal and A. S. Dhar, “Digital controlled analog architecture for DCT and DST using capacitor switching”, *Proc. Int. Symp. Circuits Systs.*, Vancouver, Canada, pp. 309 - 312, 23-26 May 2004.

22. A. K. Mal, A. Basu and A. S. Dhar, “Sampled analog architecture for DCT and DST”, *Proc. Int. Symp. Circuits Systs.*, Vancouver, Canada, pp. 825 - 828, 23-26 May 2004.

23. M. Sarma, D. Samanta and A. S. Dhar, “Motion estimation using multiresolution based on Haar wavelet transform”, *Proc. IEEE Region* 10 *Conf. Convergent Technol. Asia- Pacific* (*TENCON*), Chiang Mai, Thailand, pp. 247 - 250, 21-24 Nov. 2004.

24. A. Basu and A. S. Dhar, “Design issues in switched capacitor ladder filters”, *Proc.* 18*th Int. Conf. VLSI Design*, Kolkata, INDIA, pp. 862 - 865, 3-7 Jan. 2005.

25. R. Mahapatra, A. S. Dhar and D. Datta, “On VLSI implementation of a novel phase-shifting scheme for link adaptation in wireless communication systems”, *Nat. Conf. Commun.* (*NCC*), Kharagpur, INDIA, pp. 415 - 418, 28-30 Jan. 2005.

26. R. Mahapatra, A. S. Dhar and D. Datta, “Dynamic capacity allocation for voice and data using adaptive modulation in wireless networks”, *Proc. Int. Conf. Wireless Opt. Commun. Networks*, Bangalore, INDIA, pp. 1 - 4, 11-13 Apr. 2006.

27. C. Thakkar and A. S. Dhar, “Sampled analog architecture for 2D-DCT”, *Proc. Int. Symp. Circuits Systs.*, Greece, pp. 2369 - 2372, 21-24 May 2006.

28. K. C. Ray and A. S. Dhar, “CORDIC based VLSI architecture for Hanning and Hamming windowing for real time spectral analysis”, *Proc. Int. Conf. Comput. Devices Commun.* (*CODEC*), Kolkata, INDIA, pp.154 - 157, 18-20 Dec. 2006.

29. K. C. Ray and A. S. Dhar, “ASIC architecture for implementing Blackman windowing for real time spectral analysis”, *Proc. Int. Conf. Signal Process. Commun. Networking* (*ICSCN*), Chennai, INDIA, pp. 390 - 393, 22-24 Feb. 2007.

30. V. V. R. Teja, K. C. Ray, I. Chakraborty and A. S. Dhar, “High throughput VLSI architecture for one dimensional digital median filter”, *Proc. Int. Conf. Signal Process. Commun. Networking* (*ICSCN*), Chennai, INDIA, pp. 339 - 344, 4-6 Jan. 2008.

31. K. C. Ray, R. Teja, A. S. Dhar and I. Chakraborty, “Fast and flexible VLSI architecture for one dimensional median filter”, *Proc. Int. Conf. RF Signal Process. Syst.* (*RSPS*), Guntur, INDIA, pp. 75 - 80, 1-2 Feb. 2008.

32. B. Lakshmi and A. S. Dhar, “High speed architectural implementation of CORDIC algorithm”, *Proc. IEEE Region 10 Conf.* (*TENCON*), Hyderabad, INDIA, pp. 1 - 5, 19 - 21 Nov. 2008.

33. B. Lakshmi and A. S. Dhar, “Low latency VLSI architecture for the radix-4 CORDIC algorithm”, *Proc. IEEE Region 10 and Third Intl. Conf. Indust. Info. Syst.*, (*ICIIS*), Kharagpur, INDIA, pp. 1 - 5, 8 - 10 Dec. 2008.

34. B. Lakshmi and A. S. Dhar, “FPGA implementation of a high speed VLSI architecture for CORDIC”, *Proc. IEEE Region 10 Conf.* (*TENCON*), Singapore, pp. 1 - 5, 23-26 Nov. 2009.

35. A. Mazumdar and A. S. Dhar, “VLSI implementation of discrete Mellin transform for real time scale analysis of images”, *Proc. IEEE Region 10 Conf.* (*TENCON*), Singapore, pp. 1 - 6, 23-26 Nov. 2009.

36. A. Mazumdar and A. S. Dhar, “VLSI architecture for separable Mellin transform”, *Proc. Annual IEEE India Conf.* (*INDICON*), Ahmedabad, Gujarat, INDIA, pp. 1 - 5, 18-20 Dec. 2009.

37. M. V. N. V. Prasad, K. C. Ray and A. S. Dhar, “FPGA implementation of discrete fractional Fourier transform”, *Int. Conf. Signal Process. Commun.* (*SPCOM*), Bangalore, INDIA, pp. 1 - 5, 18-21 Jul. 2010.

38. K. C. Ray, R. Shukla and A. S. Dhar, “CORDIC-based VLSI architecture for implementing log-polar transformation for real time applications”, *Proc. Int. Conf. Computing Commun. Networking Technol.* (*ICCCNT*), Karur, Tamilnadu, INDIA, pp. 1 - 4, 29-31 Jul. 2010.

39. A. K. Mal and A. S. Dhar, “Modified Elmore delay model for VLSI interconnect”, *Proc. 53rd IEEE Int. Midwest Symp. Circuits Systs.* (*MWSCAS*), Seattle, Washington, pp. 793 - 796, 1-4 Aug. 2010.

40. B. Lakshmi and A. S. Dhar, “Parallel CORDIC-like architecture: For fast rotation implementation”, *Proc. IEEE Region 10 Conf.* (*TENCON*), Bali, Indonesia, pp. 701 - 705, 21-24 Nov. 2011.

41. N. Chattaraj and A. S. Dhar, “Random Access Analog Memory (RA^2M) for video signal application”, *Proc.* 25*th Int. Conf. VLSI Design*, Hyderabad, India, pp. 39 - 44, 7-11 Jan. 2012.

42. A. Mukherjee and A. S. Dhar, “Design of a fault-tolerant conditional sum adder”, Proc. VDAT 2012, LNCS 7373, pp. 217 - 222.

43. S. Sarkar and A. S. Dhar, “VLSI architectural design of zoomable real time spectrum analyzer”, *Proc. Annual IEEE India Conf.* (*INDICON*), Kochi, Kerala, INDIA, pp. 065 - 069, 7-9 Dec. 2012.

44. A. S. Reddy and A. S. Dhar, “Sampled analog VLSI architecture using OP-AMP based switched capacitor circuits to implement discrete Haar wavelet transform”, *Proc. Int. Conf. Emerging Technol. Trends Electron., Commun. Networking*, Surat, India, pp. 40 - 45, 19-22 Dec. 2012.

45. A. S. Reddy and A. S. Dhar, “Sampled analog VLSI architecture to implement discrete Daubechies wavelet transform”, *Proc. Int. Conf. Emerging Technol. Trends Electron., Commun. Networking*, Surat, India, pp. 46 - 51, 19-22 Dec. 2012.

46. A. Mukherjee and A. S. Dhar, “Design of a self-reconfigurable adder for fault-tolerant VLSI architecture”, *Proc. Int. Symp. Electronic System Design*, Kolkata, India, pp. 92 - 96, 19-22 Dec. 2012.

47. M. Panigrahy, I. Chakrabarti and A. S. Dhar, “VLSI design of fast fractal image encoder”, *Proc. Int. Symp. VLSI Design Test*, Coimbatore, India, pp. 1 - 2, 16-18 Jul. 2014.

48. A. Mukherjee and A. S. Dhar, “New triple-transistor based defect-tolerant systems for reliable digital architectures”, *Proc. Int. Symp. Circuits Systs.*, Lisbon, Portugal, pp. 1917 - 1920, 24-27 May 2015.